ANNA UNIVERSITY, CHENNAI
NON - AUTONOMOUS COLLEGES AFFILIATED ANNA UNIVERSITY
M.E. APPLIED ELECTRONICS
REGULATIONS – 2021
CHOICE BASED CREDIT SYSTEM

1. **PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):**

- To enable graduates to develop solutions to real world problems in the frontier areas of Applied Electronics.
- To enable the graduates to adapt to the latest trends in technology through self-learning and to pursue research to meet out the demands in industries and Academia.
- To enable the graduates to exhibit leadership skills and enhance their abilities through lifelong learning.
- To become entrepreneurs to develop indigenous solutions.

2. **PROGRAM OUTCOMES (POs)**

1.	An ability to independently carry out research/investigation and development work to solve practical problems
2.	An ability to write and present a substantial technical report/document
3.	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
4.	To critically evaluate the design and provide optimal solutions to problem areas in advanced signal processing, Consumer and automotive systems, embedded systems and VLSI design.
5.	To enhance and develop electronic systems, protocols between circuits using modern engineering hardware and software tools.
6.	To acquire knowledge of fundamentals of power electronics, power management, wireless, power supply circuits, RF circuits and FPGA circuits

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I TO IV SEMESTERS CURRICULA AND SYLLABI
SEMESTER I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	MA4101	Applied Mathematics for Electronics Engineers	FC	3	1	0	4	4
2.	RM4151	Research Methodology and IPR	RMC	2	0	0	2	2
3.	AP4151	Advanced Digital Signal Processing	PCC	3	0	0	3	3
4.	AP4152	Advanced Digital System Design	PCC	3	0	2	5	4
5.	AP4153	Semiconductor Devices and Modeling	PCC	3	0	0	3	3
6.	VL4152	Digital CMOS VLSI Design	PCC	3	0	0	3	3
7.		Audit Course – I*	AC	2	0	0	2	0
PRACTICALS								
8.	AP4111	Electronics System Design Laboratory	PCC	0	0	3	3	1.5
9.	AP4112	Signal Processing Laboratory	PCC	0	0	3	3	1.5
			TOTAL	**19**	**1**	**8**	**28**	**22**

*Audit course is optional

SEMESTER II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	AP4201	Analog and Mixed Signal IC Design	PCC	3	0	0	3	3
2.	AP4251	Industrial Internet of Things	PCC	3	0	0	3	3
3.	AP4202	Power Conversion Circuits for Electronics	PCC	3	0	0	3	3
4.	AP4203	Embedded Systems	PCC	3	0	2	5	4
5.		Professional Elective I	PEC	3	0	0	3	3
6.		Professional Elective II	PEC	3	0	0	3	3
7.		Audit Course – II*	AC	2	0	0	2	0
PRACTICALS								
8.	AP4211	VLSI Design Laboratory	PCC	0	0	4	4	2
9.	AP4212	Mini Project with seminar	EEC	0	0	2	2	1
			TOTAL	**20**	**0**	**8**	**28**	**22**

*Audit course is optional

SEMESTER III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.		Professional Elective III	PEC	3	0	0	3	3
2.		Professional Elective IV	PEC	3	0	0	3	3
3.		Professional Elective V	PEC	3	0	2	5	4
4.		Open Elective	OEC	3	0	0	3	3
PRACTICALS								
5.	AP4311	Project Work I	EEC	0	0	12	12	6
			TOTAL	**12**	**0**	**14**	**26**	**19**

SEMESTER IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICALS								
1.	AP4411	Project Work II	EEC	0	0	24	24	12
			TOTAL	**0**	**0**	**24**	**24**	**12**

TOTAL NO. OF CREDITS:75

PROFESSIONAL ELECTIVES
SEMESTER II, ELECTIVE I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	AP4001	Applications Specific Integrated Circuits	PEC	3	0	0	3	3
2.	AP4071	Computer Architecture and Parallel Processing	PEC	3	0	0	3	3
3.	AP4091	Automotive Electronics	PEC	3	0	0	3	3
4.	AP4094	Robotics	PEC	3	0	0	3	3
5.	VL4092	Soft Computing and Optimization Techniques	PEC	3	0	0	3	3

SEMESTER II, ELECTIVE II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	CU4251	RF System Design	PEC	3	0	0	3	3
2.	EL4071	Electromagnetic Interference and Compatibility	PEC	3	0	0	3	3
3.	AP4003	VLSI Design Techniques	PEC	3	0	0	3	3
4.	AP4004	Nano Technologies	PEC	3	0	0	3	3
5.	VL4252	VLSI Testing	PEC	3	0	0	3	3
6.	AP4092	Edge Analytics and Internet of Things	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	AP4093	Quantum Computing	PEC	3	0	0	3	3
2.	CU4076	VLSI for Wireless Communication	PEC	3	0	0	3	3
3.	AP4005	Micro Electro Mechanical Systems	PEC	3	0	0	3	3
4.	AP4006	Hardware Secure Computing	PEC	3	0	0	3	3
5.	VL4072	CAD for VLSI Design	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	AP4073	Sensors and Actuators	PEC	3	0	0	3	3
2.	AP4095	Signal Integrity for High Speed Design	PEC	3	0	0	3	3
3.	AP4007	Consumer Electronics	PEC	3	0	0	3	3
4.	AP4008	Advanced Microprocessors and Microcontrollers Architectures	PEC	3	0	0	3	3
5.	AP4009	Biomedical Signal Processing	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE V

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	AP4010	Modeling and Synthesis with HDL	PEC	3	0	2	5	4
2.	IF4071	Deep Learning	PEC	3	0	2	5	4
3.	AP4011	Advanced Digital Image Processing	PEC	3	0	2	5	4
4.	AP4072	PCB Design	PEC	3	0	2	5	4

AUDIT COURSES (AC)

Registration for any of these courses is optional to students

SL. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS
			L	T	P	
1.	AX4091	English for Research Paper Writing	2	0	0	0
2.	AX4092	Disaster Management	2	0	0	0
3.	AX4093	Constitution of India	2	0	0	0
4.	AX4094	நற்றமிழ் இலக்கியம்	2	0	0	0

FOUNDATION COURSES (FC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	MA4101	Applied Mathematics for Electronics Engineers	3	1	0	4	I

PROFESSIONAL CORE COURSES (PCC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	AP4151	Advanced Digital Signal Processing	3	0	0	3	I
2.	AP4152	Advanced Digital System Design	3	0	2	4	I
3.	AP4153	Semiconductor Devices and	3	0	0	3	I
4.	VL4152	Digital CMOS VLSI Design	3	0	0	3	I
5.	AP4111	Electronics System Design Laboratory	0	0	3	1.5	I
6.	AP4112	Signal Processing Laboratory	0	0	3	1.5	I

7.	AP4201	Analog and Mixed Signal IC Design	3	0	0	3	II
8.	AP4251	Industrial Internet of Things	3	0	0	3	II
9.	AP4202	Power Conversion Circuits for Electronics	3	0	0	3	II
10.	AP4203	Embedded Systems	3	0	2	4	II
11.	AP4211	VLSI Design Laboratory	0	0	4	2	II

RESEARCH METHODOLOGY AND IPR COURSES (RMC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	RM4151	Research Methodology and IPR	2	0	0	2	1

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	AP4212	Mini Project with seminar	0	0	2	1	II
2.	AP4311	Project Work I	0	0	12	6	III
3.	AP4411	Project Work II	0	0	24	12	IV

SUMMARY

Sl. No.	NAME OF THE PROGRAMME: M.E. APPLIED ELECTRONICS						
	SUBJECT AREA	CREDITS PER SEMESTER				CREDITS TOTAL	
		I	II	III	IV		
1.	FC	04	00	00	00	04	
2.	PCC	16	15	00	00	31	
3.	PEC	00	06	10	00	16	
4.	RMC	02	00	00	00	02	
5.	OEC	00	00	03	00	03	
6.	EEC	00	01	06	12	19	
7.	Non Credit/Audit Course	✓	✓	00	00		
8.	**TOTAL CREDIT**	**22**	**22**	**19**	**12**	**75**	

MA4101 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS L T P C
3 1 0 4

COURSE OBJECTIVES:

- To introduce the fundamentals of fuzzy logic.
- To understand the basics of random variables with emphasis on the standard discrete and continuous distributions.
- To understand the basic probability concepts with respect to two dimensional random variables.
- To make students understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete – time Markov chains.
- To provide the required fundamental concepts in queueing models and apply these techniques in networks, image processing.

UNIT I FUZZY LOGIC 12

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy qualifiers.

UNIT II PROBABILITY AND RANDOM VARIABLES 12

Probability – Axioms of probability – Conditional probability – Bayes theorem – Random variables – Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a random variable.

UNIT III TWO DIMENSIONAL RANDOM VARIABLES 12

Joint distributions – Marginal and conditional distributions – Functions of two dimensional random variables – Regression curve – Correlation.

UNIT IV RANDOM PROCESSES 12

Classification – Stationary random process – Markov process – Markov chain – Poisson process – Gaussian process - Auto correlation – Cross correlation.

UNIT V QUEUEING MODELS 12

Poisson process – Markovian queues – Single and multi server models – Little's formula – Machine Interference model – Steady state analysis – Self service queue.

TOTAL : 60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

- apply the concepts of fuzzy sets, fuzzy logic, fuzzy prepositions and fuzzy quantifiers and in relate.
- analyze the performance in terms of probabilities and distributions achieved by the determined solutions.
- use some of the commonly encountered two dimensional random variables and extend to multivariate analysis.
- classify various random processes and solve problems involving stochastic processes.
- use queueing models to solve practical problems.

REFERENCES:

1. Ganesh M., “Introduction to Fuzzy Sets and Systems, Theory and Applications”, Academic Press, New York, 1997.
2. George J. Klir and Yuan B,” Fuzzy sets and Fuzzy logic” Prentice Hall, New Delhi, 2006.
3. Devore J.L, “Probability and Statistics for Engineering and Sciences”, Cengage learning, 9th Edition, Boston, 2017.
4. Johnson R.A. and Gupta, C.B., “ Miller and Freunds Probability and Statistics for Engineers”, Pearson India Education, Asia, 9th Edition, New Delhi, 2017.
5. Oliver C. Ibe,” Fundamentals of applied probability and Random process”, Academic press, Boston, 2014.
6. Gross D. and Harris C.M., “Fundamentals of Queuing theory”, Willey student, 3rd Edition, New Jersey, 2004.

RM4151 RESEARCH METHODOLOGY AND IPR L T P C
2 0 0 2

UNIT I RESEARCH DESIGN 6

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

UNIT II DATA COLLECTION AND SOURCES 6

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.

UNIT III DATA ANALYSIS AND REPORTING 6

Overview of Multivariate analysis, Hypotheses testing and Measures of Association.
Presenting Insights and findings using written reports and oral presentation.

UNIT IV INTELLECTUAL PROPERTY RIGHTS 6

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT V PATENTS 6

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.

TOTAL:30 PERIODS

REFERENCES

1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education, 11e (2012).
2. Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007.

3. David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
4. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.

AP4151 ADVANCED DIGITAL SIGNAL PROCESSING L T P C
3 0 0 3

COURSE OBJECTIVES:

- To describe fundamental concepts of DSP and Discrete Transforms
- To design digital filters design
- To estimate power spectrum using non- parametric and parametric methods
- To analyze the Multirate Signal processing by decimation and interpolation.
- To apply the concept of multirate signal processing for various applications

UNIT I DIGITAL SIGNAL PROCESSING 9

Sampling of analog signals - Selection of sampling frequency - Frequency response - Transfer functions - Filter structures - Fast Fourier Transform (FFT) Algorithms - Image coding - DCT.

UNIT II DIGITAL FILTER DESIGN 9

IIR and FIR Filters: Filter structures, Implementation of Digital Filters - 2nd Order Narrow Band Filter and 1st Order All Pass Filter, Frequency sampling structures of FIR, Lattice structures, Forward and Backward prediction error filters, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT III ESTIMATION OF POWER SPECTRUM 9

Non-Parametric Methods: Estimation of spectra from finite duration observation of signals,: Bartlett, Welch & Blackman-Tukey methods, Performance Comparison. Parametric Methods: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT IV MULTI RATE SIGNAL PROCESSING 9

Decimation by a factor D - Interpolation by a factor I - Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design and Implementation for sampling rate conversion. Up-sampling using All Pass Filter.

UNIT V APPLICATIONS OF MULTI RATE SIGNAL PROCESSING AND DSP INTEGRATED CIRCUITS 9

Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Subband Coding of Speech Signals, Quadrature Mirror Filters, Over Sampling A/D and D/A Conversion.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will be able to

CO1: Describe the basics of Digital Signal Processing and Discrete Time Transforms.

CO2. Design and implement FIR/IIR digital filters using various structures

CO3. Estimate power spectrum using appropriate parametric/non-parametric method.

CO4: Analyze discrete time system at different sampling frequencies using the concept of Multirate signal processing

CO5: Design discrete time system for the given application using Multi rate signal processing

REFERENCES:

1. J.G.Proakis & D. G.Manolakis Digital Signal Processing: Principles, Algorithms & Applications -, 4th Ed., Pearson Education, 2013.
2. Alan V Oppenheim & Ronald W Schaffer Discrete Time signal processing, Pearson Education, 2014.
3. Keshab K. Parhi, 'VLSI Digital Signal Processing Systems Design and Implementation", John Wiley& Sons, 2007.
4. Steven. M .Kay, Modern Spectral Estimation: Theory & Application –PHI, 2009.
5. P.P.Vaidyanathan, Multi Rate Systems and Filter Banks , Pearson Education, 1993.
6. Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital Signal Processing–A practical approach", Second Edition, Harlow, Prentice Hall, 2011.

AP4152 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 2 4

COURSE OBJECTIVES:

- To design asynchronous sequential circuits.
- To learn about hazards in asynchronous sequential circuits.
- To study the fault testing procedure for digital circuits.
- To understand the architecture of programmable devices.
- To design and implement digital circuits using programming tools.

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Circuits and Modelling- State Diagram, State Table, State Table Assignment and Reduction-Design of Synchronous Sequential Circuits Design of Iterative Circuits-ASM Chart and Realization using ASM.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit – Flow Table Reduction-Races-State Assignment-Transition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards – Mixed Operating Mode Asynchronous Circuits – Designing Vending Machine Controller.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method-Path Sensitization Method – Boolean Difference Method - D Algorithm –– Tolerance Techniques – The Compact Algorithm – Fault in PLA – Test Generation - DFT Schemes – Built in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming Logic Device Families – Designing a Synchronous Sequential Circuit using PLA/PAL – Designing ROM with PLA – Realization of Finite State Machine using PLD – FPGA – Xilinx FPGA - Xilinx 4000.

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types And Operators For Modelling

In Verilog HDL - Behavioural Descriptions In Verilog HDL – HDL Based Synthesis – Synthesis Of Finite State Machines– Structural Modelling – Compilation And Simulation Of Verilog Code – Test Bench - Realization Of Combinational And Sequential Circuits Using Verilog – Registers – Counters – Sequential Machine – Serial Adder – Multiplier- Divider – Design Of Simple Microprocessor, Introduction To System Verilog.

45 PERIODS

SUGGESTED ACTIVITIES:

1: Design asynchronous sequential circuits.
2: Design synchronous sequential circuits using PLA/PAL.
3: Simulation of digital circuits in FPGA.
4: Design digital systems with System Verilog.

PRACTICAL EXERCISES: **30 PERIODS**

1. Design of Registers by Verilog HDL.
2. Design of Counters by Verilog HDL.
3. Design of Sequential Machines by Verilog HDL.
4. Design of Serial Adders , Multiplier and Divider by Verilog HDL.
5. Design of a simple Microprocessor by Verilog HDL.

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Analyse and design synchronous sequential circuits.
CO2: Analyse hazards and design asynchronous sequential circuits.
CO3: Knowledge on the testing procedure for combinational circuit and PLA.
CO4: Able to design PLD and ROM.
CO5: Design and use programming tools for implementing digital circuits of industry standards.

TOTAL:75 PERIODS

REFERENCES

1. Charles H.Roth jr., “Fundamentals of Logic Design” Thomson Learning,2013.
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001.
5. Paragk.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
6. Paragk.Lala “Digital System Design Using PLD” B S Publications,2003.
7. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

AP4153 SEMICONDUCTOR DEVICES AND MODELING **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To acquire the fundamental knowledge and to expose to the field of semiconductor theory and devices and their applications.
- To gain adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications

- To acquire the fundamental knowledge of different semiconductor device modelling aspects.

UNIT I MOS CAPACITORS 9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–OxideInterface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown.

UNIT II MOSFET DEVICES 9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields

UNIT III CMOS DEVICE DESIGN 9

CMOS Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements.

UNIT IV BIPOLAR DEVICES 9

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor.

UNIT V MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of this course, the students will be able to

CO1: Explore the properties of MOS capacitors.

CO2: Analyze the various characteristics of MOSFET devices.

CO3: Describe the various CMOS design parameters and their impact on performance of the device.
CO4: Discuss the device level characteristics of BJT transistors.
CO5: Identify the suitable mathematical technique for simulation.

REFERENCES:

1. Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.
2. A.B. Bhattacharyya “Compact MOSFET Models for VLSI Design”, John Wiley & Sons Ltd, 2009.
3. Ansgar Jungel, “Transport Equations for Semiconductors”, Springer, 2009
4. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2004
5. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag., 1984
6. Behzad Razavi, “Fundamentals of Microelectronics” Wiley Student Edition, 2nd Edition, 2014
7. J P Collinge, C A Collinge, “Physics of Semiconductor devices” Springer, 2002.
8. S.M.Sze, Kwok.K. NG, “Physics of Semiconductor devices”, Springer, 2006.

VL4152 **DIGITAL CMOS VLSI DESIGN** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To introduce the transistor level design of all digital building blocks common to all cmos microprocessors, network processors, digital backend of all wireless systems etc.
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, elmore constant , CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS 9

Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.

UNIT V MEMORY ARCHITECTURES 6

Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-

Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Use mathematical methods and circuit analysis models in analysis of CMOS digital circuits

CO2: Create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort

CO3: Design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches

CO4: Understand design methodology of arithmetic building blocks

CO5: Design functional units including ROM and SRAM

TOTAL:45 PERIODS

REFERENCES:

1. N.Weste, K. Eshraghian, " Principles Of Cmos VLSI Design", Addision Wesley, 2nd Edition, 1993
2. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
3. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design", Mcgraw-Hill, 1998
4. Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective", Prentice Hall Of India, 2nd Edition, Feb 2003

AP4111	ELECTRONICS SYSTEM DESIGN LABORATORY	L	T	P	C
		0	0	3	1.5

COURSE OBJECTIVES:

- Design of instrumentation amplifier and voltage regulator
- Design of PCB layout
- Write a Verilog HDL coding of various combinational circuits
- Verify the design functionality for various memory modules
- Design of PLL circuits

LIST OF EXPERIMENTS:

1. Design of a 4-20 mA transmitter for a bridge type transducer.

   Design the Instrumentation amplifier with the bridge type transducer (Thermistor or any resistance variation transducers) and convert the amplified voltage from the instrumentation amplifier to 4 – 20 mA current using op-amp. Plot the variation of the temperature Vs output current.

2. Design of AC/DC voltage regulator using SCR

   Design a phase controlled voltage regulator using full wave rectifier and SCR, vary the conduction angle and plot the output voltage.

3. PCB layout design using CAD

Drawing the schematic of simple electronic circuit and design of PCB layout using CAD

4. HDL based design entry and simulation of Parameterizable cores of Counters, Shift registers, State machines, 8-bit Parallel adders and 8 –Bit multipliers.

5. HDL based design entry and simulation of Parameterizable cores on the simple Distributed Arithmetic system. Test vector generation and timing analysis.

6. HDL based design entry and simulation of Parameterizable cores on memory design and 4 – bit ALU. Synthesis, P&R and post P&R simulation, Critical paths and static timing analysis results to be identified. FPGA real time programming and I/O interfacing.

7. Interfacing with Memory modules in FPGA Boards. Verifying design functionality by probing internal signals.

8. Realization of Discrete Fourier transform/Fast Fourier Transform algorithm in HDL and observing the spectrum in simulation.

9. Invoke PLL module and demonstrate the use of the PLL for clock generation in FPGAs. Verify design functionality implemented in FPGA by capturing the signal in Oscilloscope

TOTAL :45 PERIODS

COURSE OUTCOMES:

CO1: Design an instrumentation amplifier and voltage regulator
CO2: Design a PCB layout using CAD tool
CO3: Write a Verilog code for various combinational and sequential circuits
CO4: Develop a memory module with FPGA
CO5: Design an PLL circuit

REFERENCES:

1. Neil H.E. Weste, David Harris, Ayan Banerjee, “CMOS VLSI Design- A circuits and Systems Perspective”, Third Edition, 2013, Pearson education.
2. M. Morris Mano, Michael D. Ciletti, “Digital Design with an introduction to Verilog HDL”, PHI, 6th Edition, 2018
3. James E. Palmer, David E. Perlman,``Schuams Outlines-Introduction to Digital Systems”, Tata McGraw Hill, 2nd Edition 2003
4. Sergio Franco, “Design with operational amplifiers and analog integrated circuits”, 3rd Edition, Tata McGraw Hill, 2007
5. D.Roy Choudhry, Shail Jain, “Linear Integrated Circuits”, New Age International Private Limited, 4th Edition, 2010

AP4112	SIGNAL PROCESSING LABORATORY	L T P C 0 0 3 1.5

COURSE OBJECTIVES:

- To provide the student with the basic understanding of audio signal analysis using filters
- To provide the students with the understanding of the working of statistical method based approaches
- To impart the students with the design of filters
- To demonstrate the working of algorithms for different applications
- To provide knowledge of analyzing the images and video

LIST OF EXPERIMENTS:

1. Design of Adaptive channel equalizer
2. Realization of sub band filter using linear convolution
3. Realization of STFT using FFT
4. Demonstration of Bayes technique
5. Demonstration of Min-max technique
6. Realization of FIR Wiener filter
7. Generation of Multivariate Gaussian generated data with desired mean vector and the required co-variance matrix.
8. Design and Realization of the adaptive filter using LMS algorithm (solved using steepest-descent algorithm)
9. Representation of the 2D image signal as the linear combinations of PCA (Eigen faces)
10. Image compression using Discrete cosine transformation (DCT).
11. Multiple-input Multiple output (MIMO)
12. Speech recognition using Support Vector Machine (SVM)
13. LMS filtering implementation using TMS320C6x processor
14. Face detection and tracking in video using OpenCV

TOTAL :45 PERIODS

COURSE OUTCOMES:

CO1: Obtain the ability to apply knowledge of linear algebra, random process and multirate signal processing in various signal processing applications.

CO2: Develop the student's ability on conducting engineering experiments, analyze experimental observations scientifically

CO3: Become familiar to fundamental principles of linear algebra

CO4: Familiarize the basic operations of filter banks through simulations

CO5: Apply the principles of random process in practical applications

REFERENCES

1. Vinay K.Ingle,John G.Proakis, Digital signal processing using MATLAB, Cengage Learning, 3rd edition, 2011
2. Michael R King, Nipa Mody, Numerical and statistical methods for Bio Engineering – Applications using MATLAB , CAMBRIDGE University Press, 2010
3. V. Siahaan, R.H.Sianipar, Signal and Image processing with python GUI, Balige Publishing,2021

AP4201	ANALOG AND MIXED SIGNAL IC DESIGN	L T P C 3 0 0 3

COURSE OBJECTIVES:

- To study the concepts of MOS large signal model and small signal model
- To provide in-depth understanding of the analog integrated circuit and building blocks
- To learn the Analog and Digital layout design for mixed signal circuits
- To Understand the methodologies for analysis and design of fundamental CMOS Analog and Mixed signal Circuits like Data Converters and filters.
- To study the integrated circuits like oscillators and PLLs.

UNIT I INTRODUCTION AND BASIC MOS DEVICES 9

Challenges in analog design-Mixed signal layout issues- MOS FET structures and characteristics- large signal model – small signal model- single stage Amplifier-Source follower-Common gate stage – Cascode Stage

UNIT II SUBMICRON CIRCUIT DESIGN 9

Submicron CMOS process flow, Capacitors and resistors, Current mirrors, The MOSFET Switch, Analog Circuit Design: Biasing, Op-Amp Design, Circuit Noise - OP Amp parameters

UNIT III DATA CONVERTERS 9

Characteristics of Sample and Hold- Digital to Analog Converters- architecture-Differential Non linearity-Integral Non linearity- Voltage Scaling-Cyclic DAC-Pipeline DAC-Analog to Digital Converters- architecture – Flash ADC-Pipeline ADC-Differential Non linearity-Integral Non linearity. Overview of SNR of Data Converters- Clock Jitters- Improving Using Averaging – Decimating Filters for ADC- Band pass and High Pass Sinc Filters- Interpolating Filters for DAC

UNIT IV ANALOG AND DIGITAL LAYOUT DESIGN FOR MIXED SIGNAL 9

Layout introduction: Introduction, MOS transistor layers, stick diagram, symbolic diagram. Digital layout design: Introduction, guide line of transistor layout, PMOS and NMOS transistor layout, CMOS transistor layout. Introduction to analog layout techniques and Passive component layout - capacitor, resistor and inductor, Floor planning of analog and digital components, power supply and ground pin issues, matching, shielding, interconnection issues.

UNIT V OSCILLATORS AND PLL 9

LC oscillators, Voltage Controlled Oscillators. Simple PLL, Charge pumps PLLs, Non ideal effects in PLLs, Delay Locked Loops. Applications of PLL.frequency multiplication and synthesis. Introduction to RF IC Design, building blocks, applications.

SUGGESTED ACTIVITIES:

ICT/MOOCs Reference :
https://nptel.ac.in/courses/117/101/117101105/

COURSE OUTCOMES:

At the end of this course the students will be able to:

CO1: Carry out research and development in the area of analog and mixed signal IC design.
CO2: Well versed with the MOS fundamentals, small signal models and analysis of MOSFET based circuits.
CO3 Analyse and model data converters architecture
CO4: Understand and Design different mixed signal circuits for various applications as per the user specifications.
CO5: Analyze and design mixed signal circuits such as Comparator, ADCs, DACs, PLL.

TOTAL : 45 PERIODS

REFERENCES

1. P. Allen and D. Holberg, "CMOS Analog Circuit Design", Oxford University Press, Second Edition, 2012.
2. B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2003.
3. R.Jacob Baker,H.W.Li, and D.E. Boyce CMOS Circuit Design ,Layout and Simulation, Prentice-Hall of India,1998.
4. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley Publishers, Fifth Edition, 2009.

AP4251 INDUSTRIAL INTERNET OF THINGS L T P C
3 0 0 3

COURSE OBJECTIVES:

- To understand the fundamentals of Internet of Things
- To learn about the basics of IOT protocols
- To build a small low cost embedded system using IoT
- To apply the concept of I0T in the real world scenario

UNIT I INTRODUCTION AND ARCHITECTURE OF IoT 9

Introduction – Definition and characteristics of IoT – Physical and Logical Design of IoT - Communication models and APIs – Challenges in IoT - Evolution of IoT- Components of IoT - A Simplified IoT Architecture – Core IoT Functional Stack.

UNIT II INDUSTRIAL IoT 9

IIoT-Introduction, Industrial IoT: Business Model and Reference Architecture: IIoT-Business Models, Industrial IoT- Layers: IIoT Sensing, IIoT Processing, IIoT Communication, IIoT Networking

UNIT III IIOT ANALYTICS 9

Big Data Analytics and Software Defined Networks, Machine Learning and Data Science, Julia Programming, Data Management with Hadoop

UNIT IV IOT SECURITY 9

Industrial IoT: Security and Fog Computing - Cloud Computing in IIoT, Fog Computing in IIoT, Security in IIoT

UNIT V CASE STUDY 9

Industrial IOT- Application Domains: Oil, chemical and pharmaceutical industry, Applications of UAVs in Industries, Real case studies: Milk Processing and Packaging Industries, Manufacturing Industries

TOTAL : 45 PERIODS

COURSE OUTCOMES:

Upon completion of this course, student will be able to

CO1: Understand the basic concepts and Architectures of Internet of Things.

CO2: Understand various IoT Layers and their relative importance.

CO3: Realize the importance of Data Analytics in IoT.

CO4: Study various IoT platforms and Security

CO5: Understand the concepts of Design Thinking.

REFERENCE BOOKS

1. Industry 4.0: The Industrial Internet of Things", by Alasdair Gilchrist (Apress), 2017
2. "Industrial Internet of Things: Cybermanufacturing Systems"by Sabina Jeschke, Christian Brecher, Houbing Song, Danda B. Rawat (Springer), 2017
3. Hands-On Industrial Internet of Things: Create a powerful Industrial IoT by Giacomo Veneri, Antonio Capasso, Packt, 2018.

AP4202 POWER CONSERVATION CIRCUITS FOR ELECTRONICS L T P C

3 0 0 3

COURSE OBJECTIVE:

- To provide the students a deep insight in to the working of different switching devices with respect to their characteristics
- To analyze different converters with their applications.
- To study advanced converters and switching techniques implemented in recent technology

UNIT I POWER ELECTRONIC DEVICES AND SEMICONDUCTOR SWITCHES 9

Introduction, Applications of power electronics, Power electronics devices: Characteristics of power devices – characteristics of SCR, diac, triac, GTO, PUJT, power transistors – power FETs – LASCR – two transistor model of SCR Protection of thyristors against over voltage – over current, dv/dt and di/dt. Power Semiconductor Switches: Rectifier diodes, fast recovery diodes.

UNIT II SCR PERFORMANCE AND APPLICATIONS 9

Turn on circuits for SCR – triggering with single pulse and train of pulses synchronizing with supply – Thyristor turn off methods, natural and forced commutation, self-commutation series and parallel operations of SCRs. Rectifiers: Single phase and three phase controlled Rectifiers with inductive loads, RL load. Construction & Working of Opto- Isolators, Opto-TRIAC, Opto-SCR.

UNIT III INVERTERS AND VOLTAGE CONTROLLERS 9

Voltage and current source inverters, resonant, Series inverter, PWM inverter. AC and DC choppers – DC to DC converters – Buck, boost and buck – boost.

Single phase and three phase Cyclo-conveters, Power factor control and Matrix Converters. Industrial applications DC and AC Drives DC Motor Speed control Induction Motor Speed Control.

UNIT IV TIMERS & DELAY ELEMENTS, HIGH FREQUENCY POWER HEATING, SENSOR AND ACTUATORS 9

RC Base Constant Timers, Timer Circuits using SCR, IC-555, Programmable Timer and their Industrial Applications, Induction Heating and Dielectric Heating System and Their Applications, Sensors, Transducers, and Transmitters for Measurement, Control & Monitoring : Thermoresistive Transducer, Photoconductive Transducers, Pressure Transducers, Flow Transducers, Level Sensors, Speed Sensing, Vibration Transducers, Variable-Frequency Drives, Stepper Motors and Servomotor Drives.

UNIT V AUTOMATION AND CONTROL 9

Data Communications for Industrial Electronics, Telemetry, SCADA & Automation, AC & DC Drives, Voltage & Power Factor Control through Solid State Devices, Soft Switching, Industrial Robots.

TOTAL :45 CREDITS

COURSE OUTCOMES:

At the end of this course students will be able to:

CO1: Describe the characteristics, operation of power switching devices and identify their ratings and applications.

CO2: Understand the requirements SCR Protection, Describe the Functioning of SCR their Construction and Performance.

CO3: Analyze and Design the Converter Based on SCR for various Industrial Applications.

CO4: Demonstrate ability to understand High Frequency, Heating Systems, Timers, Relevant Sensors & Actuator and their Application in Industrial Setting.

CO5: Demonstrate the ability to understand and apply Data Communication, Telemetry & SCADA System in Industrial Applications.

REFERENCES:

1. Thomas E. Kissell, Industrial Electronics: Applications for Programmable Controllers, Instrumentation and Process Control, and Electrical Machines and Motor Controls, 3rd edition, 2003, Prentice Hall.
2. B. Paul, Industrial Electronic and Control, Prentice Hall of India Private Limited (2004).
3. M.H. Rashid, “Power Electronics: Circuits, Devices & Applications”, Prentice Hall of India Ltd. 3rd Edition, 2004.
4. Ned Mohan, T.M. Undeland and W.P. Robbins, “Power Electronics: Converters, Applications and Design”, Wiley India Ltd, 2008.
5. M.S. Jamil Asghar, “Power Electronics” Prentice Hall of India Ltd., 2004
6. V.R. Moorthy, “Power Electronics: Devices, Circuits and Industrial Applications” Oxford University Press, 2007.
7. G.K. Dubey, Power Semiconductor Controlled Drives, Prentice Hall inc. (1989).
8. J.M.D. Murphy, F.G. Turnbull, Power Electronic Control of Ac Motors, Pergamon (1990).

AP4203 EMBEDDED SYSTEMS L T P C

3 0 2 4

COURSE OBJECTIVES:

- Learn Embedded design challenges and design methodologies
- Study general and single purpose processor

- Understand bus structures
- Design a state machine and concurrent process models
- Know about Embedded software development tools and RTOS.

UNIT I EMBEDDED SYSTEM OVERVIEW 9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR 9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer's view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES 9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS 9

Basic State Machine Model, Finite-State Machine with Datapath Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models

UNIT V EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS 9

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS.

TOTAL : 45 PERIODS

SUGGESTED ACTIVITIES:

1: Insist students to write a requirements form for a smart phone
2: Compare the use of different Microcontrollers for a particular ESD.
3: Application of a protocol for a specified application.
4: Write a Embedded C code for a given task.
5: design an embedded system for any type of real time application

PRACTICAL LIST:

Exercise – 1

Comparative study of software development tools and design steps with respect to FPGA based and Non – FPGA based (defined logic) embedded system development.

(For Example: consider any Spartan FPGA board for FPGA based Embedded System Consider any cortex- M based board for Non – FPGA based Embedded system)

Exercise – 2

Implement adder and decoder logic blocks in any one of the FPGA chip based development board.

Exercise – 3

Design and development of UART protocol logic block in any one of FPGA chip based development board.

Exercise – 4

Consider on board LEDS (any four) and timer logic block of cortex- M board. Write a program which enables LEDS to glow in different timing.

Exercise – 5

Consider on board switches and (2x16) LCD display develop a program which displays the status of switch activation.

Exercise – 6

Demonstrate GPIO based I/O interfacing by considering LM 35 temperature sensor and cortex- M board.

Exercise – 7

Development of one interfacing scheme which transmits data from one cortex- M board to another cortex- M board using on chip CAN logic blocks.

Exercise – 8

Consider on board EPROM IC of Cortex- M board by utilizing on chip I2c logic block transmit data to EPROM IC and receive stored data from EPROM IC.

Exercise – 9

Consider on board LEDs (4 Nos) of Cortex - M board. Demonstrate time management service concept of RTOS for glowing all four LEDS in different timings.

Exercise – 10

Consider two ultrasonic sensors which are interfaced with cortex- M board. Both are located some distance (2 meters) apart vertically so that the system can identify the movement of object in term of distance. consider data reception and display of each sensor as two different tasks by RTOS. Establish a RTOS based system to recognize the height of moving object.

Objective:

a. Able to understand embedded system design flow in FPGA chip based and Non – FPGA chip based embedded development boards.
b. Able to create simple logic blocks in FPGA chip based boards.
c. Able to understand interfacing scheme for Non – FPGA board scheme for Non – FPGA board
d. Able to utilize RTOS functions for interfacing practice

HARDWARE AND SOFTWARE REQUIREMENTS

1. Cortex- M board and simulation tools
2. FPGA EVM Board and simulation tools
3. Ultrasonic sensor
4. Any portable open source RTOS

COURSE OUTCOMES:

At the end of the course the student will be:

CO1: Able to design an Embedded system

CO2: Understand a general and single purpose processor

CO3: Explain different protocols

CO4: Discuss state machine and design process models
CO5: Outline embedded software development tools and RTOS

TOTAL:45+30=75 PERIODS

REFERENCES

1. Bruce Powel Douglas, “Real time UML, second edition: Developing efficient objects for embedded systems”, 3rd Edition 1999, Pearson Education.
2. Daniel W. Lewis, “Fundamentals of embedded software where C and assembly meet”, Pearson Education, 2002.
3. Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & sons, 2002.
4. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004

AP4211	VLSI DESIGN LABORATORY	L T P C 0 0 4 2

COURSE OBJECTIVE:

- Familiarize with different FPGA boards
- Analyze digital design using Front end Tools
- Analyze the CMOS circuits using CAD tools
- Analyze the interfacing of I/O devices with Arduino Boards using Embedded C

PRACTICAL EXPERIMENTS:

1. Synthesize and implement Combinational and Sequential Circuits in VERILOG / VHDL
2. Synthesize and implement MAC unit and GCD unit in Verilog /VHDL
3. Implementation of sampling of input signal and display in FPGA Synthesize and implement FIR filter and IIR filter Verilog /VHDL
4. Synthesize and implement 8 bit general purpose processor in Verilog/VHDL
5. Synthesize and implement UART and USART
6. Simulation and Analysis of CMOS combinational and sequential logic circuits using CAD tools

TOTAL : 60 PERIODS

COURSE OUTCOME:

At the end of the course, the students will be able to
CO1: Program in Verilog/VHDL for combinational and sequential circuits and implement the program in FPGA
CO2: Implement FIR and IIR filters in FPGA
CO3: Implement data path design and interfaces
CO4: Handle CAD tools to draw/edit, and analyze the CMOS circuits.
CO5: Program and interface the Arduino Boards using Embedded C

AP4001 APPLICATIONS SPECIFIC INTEGRATED CIRCUITS L T P C
3 0 0 3

COURSE OBJECTIVE:

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To analyze the issues and tools related to ASIC/FPGA design and implementation.
- To understand basics of System on Chip and Platform based design.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell -Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti-fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECTURE 9

Architecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs – Micro-Blaze / Niosbased embedded systems – Signal probing techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING 9

Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies.

UNIT V HIGH PERFORMANCE ALGORITHMS FOR ASICs/ SOCs. SOC CASE STUDIES 9

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. CaseStudies: Digital camera, SDRAM, High speed data standards.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course students will be able:

CO1: To architect ASIC library design
CO2: To develop programmable ASIC logic cells
CO3: To design I/O cells and interconnects
CO4: To understand logic synthesis, placement and routing
CO5: To identify new developments in SOC and low power design

REFERENCES:

1. Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996.
2. Jose E. France, YannisTsividis, "Design of Analog - Digital VLSI Circuits forTelecommunication and Signal Processing", Prentice Hall, 1994.
3. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2003.
4 Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994.
5 Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementationof Signal Processing Systems”, Wiley, 2008.
6 Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science,2007

AP4071 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING L T P C
3 0 0 3

COURSE OBJECTIVES:

- Discuss the basic concepts and structure of computers.
- Explain the concepts of number representation and arithmetic operations.
- Explain different types of Memory architectures.
- Describe various parallel processing schemes and vector architecture.
- Summarize the Instruction execution stages and Memory hierarchy.

UNIT I INTRODUCTION TO COMPUTER ORGANIZATION 9

Architecture and function of general computer system - Basic Operational Concepts, Bus Structures, Software Performance – Memory locations & addresses – Memory operations – Instruction and instruction sequencing – addressing modes – assembly language - System buses, Multi-bus organization

UNIT II DATA REPRESENTATION 9

Signed number representation, fixed and floating point representations, character representation. Computer arithmetic - integer addition and subtraction, ripple carry adder, carry look-ahead adder - multiplication - shift-and-add, Booth multiplier, carry save multiplier - Division - non-restoring and restoring techniques, floating point arithmetic.

UNIT III PROCESSOR ARCHITECTURE AND CONTROL UNIT 9

A Basic MIPS implementation – Building a Datapath – Control Implementation Scheme – Hardwired control – micro programmed control - Pipelining – Pipelined datapath and control – Handling Data Hazards & Control Hazards – Exceptions. Processor Architecture: Very Long Instruction Word (VLIW) Architecture, Digital Signal Processor Architecture, System on Chip (SoC) architecture, MIPS Processor and programming

UNIT IV PARALLEL PROCESSING 9

Parallel processing challenges – Flyn's classification – Single Instruction Single Data (SISD), Multiple Instruction Multiple Data (MIMD), Single Instruction Multiple Data (SIMD), Single Program Multiple Data (SPMD), and Vector Architectures - Hardware multithreading – Multi-core processors and other Shared Memory Multiprocessors - Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message-Passing Multiprocessors.

UNIT V MEMORY & I/O SYSTEMS 9

Memory Hierarchy – memory technologies – cache memory – measuring and improving cache performance – virtual memory, Translation Lookaside Buffers – Accessing I/O Devices – Interrupts – Direct Memory Access – Bus structure – Bus operation – Arbitration – Interface circuits – Universal Serial Bus.

TOTAL: 45 PERIODS

COURSE OUTCOMES

Upon completion of this course, the student will be able to

CO1: Understand the basic organization of computer and different instruction formats and addressing modes. (K2)

CO2: Interpret the representation and manipulation of data on the computer. (K3)

CO3: Illustrate about implementation schemes of control unit and pipeline performance. (K2)

CO4: Summarize the various types of parallelism architectures. (K2)

CO5: Compare the various memory hierarchy and I/O systems. (K2)

REFERENCES

1. David A. Patterson and John L. Hennessy, “Computer Organization and Design: The Hardware/Software Interface”, Morgan Kaufmann / Elsevier, 5th Edition, 2014.
2. Carl Hamacher, ZvonkoVranesic, SafwatZaky and NaraigManjikian, “Computer Organization and Embedded Systems”, Tata McGraw Hill, 6th Edition, 2012.
3. William Stallings, “Computer Organization and Architecture – Designing for Performance”, Pearson Education, 8th Edition, 2010.
4. John P. Hayes, “Computer Architecture and Organization”, Tata McGraw Hill, 3rd Edition, 2012.
5. John L. Hennessey and David A. Patterson, “Computer Architecture – A Quantitative Approach”, Morgan Kaufmann / Elsevier Publishers, 5th Edition, 2012.

AP4091 AUTOMOTIVE ELECTRONICS L T P C
3 0 0 3

COURSE OBJECTIVES:

- To explain the principle of electronic management system and different sensors used in the systems.
- To know the concepts and develop basic skills necessary to diagnose automotive electronic problems.
- To know Starting, and charging, lighting systems, advanced automotive electrical systems.
- To include electronic accessories and basic computer control.
- To explore practically about the components present in an Automotive electrical and electronics system.

UNIT I FUNDAMENTALS 9

Components for electronic engine management system, open and closed loop control strategies, PID control, Look up tables, introduction to modern control strategies like Fuzzy logic and adaptive control. Switches, active resistors, Transistors, Current mirrors/amplifiers, Voltage and current references, Comparator, Multiplier. Amplifier, filters, A/D and D/A converters.

UNIT II MODERN SENSORS 9

Film sensors, micro-scale sensors, Particle measuring systems, Vibration Sensors, SMART sensors, Machine Vision, Multi-sensor systems Applications of Sensors: Applications and case studies of Sensors in Automobile Engineering, Aeronautics, Machine tools and Manufacturing processes.

UNIT III CHARGING SYSTEM 9

Generation of Direct Current- Shunt Generator Characteristics- Armature Reaction- Third Brush Regulation- Cutout. Voltage and Current Regulators- Compensated Voltage Regulator Alternators Principle and Constructional Aspects and Bridge Rectifiers- New Developments.

UNIT IV AUTOMOTIVE TRANSMISSION CONTROL SYSTEMS 9

Transmission control - Cruise control – Braking control – Traction control –Suspension control –

Steering control – Stability control – Integrated engine control.

UNIT V ELECTRONICS SYSTEMS 9

Current Trends in Automotive Electronic Engine Management System- Types of EMS Electromagnetic interference Suppression- Electromagnetic Compatibility- Electronic Dashboard Instruments- Onboard Diagnostic System- Security - Warning System infotainment and Telematics.

TOTAL : 45 PERIODS

SUGGESTED ACTIVITIES:

1. Testing of battery, starting systems, charging systems, ignition systems and body controller systems
2. Study of various sensors and actuators used in two wheelers and four wheelers for electronic control.
3. Study of Development of Embedded Systems projects.

COURSE OUTCOMES:

At the end of this course the students will be able to:

CO1: Explain the fundamentals, operation, function of various sensors and actuators in engine management systems.

CO2: Explain the Automotive Transmission Control Systems.

CO3: Enumerate the principles, application, construction and specification of different sensors and actuators usable in typical automobile by suitable testing.

CO4: List out the principles and characteristics of charging system components and demonstrate their working with suitable tools.

CO5: Describe the principles and architecture of electronics systems and its components present in an automobile related to instrumentation, control, security and warning systems.

REFERENCES

1. Allan Bonnick, “Automotive Computer Controlled Systems”, Butterworth- Heinemann, Elsevier, I Edition, 2011.
2. Eric Chowanietz, “Automobile Electronics” by SAE Publications, 1995
3. Tom Weather Jr and Cland C. Hunter, “Automotive Computers and Control System” Prentice H Inc.,1984 New Jersey.
4. R.K. Jurgen, “Automotive Electronics Handbook”, McGraw Hill 2 nd Edition,1995.
5. William B Ribbens, “understanding automotive electronics”, 5th edition - Butter worth Heinemai Woburn, 1998.

AP4094 **ROBOTICS** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To Introduce the concepts of Robotic systems
- To understand the concepts of Instrumentation and control related to Robotics
- To understand the kinematics and dynamics of robotics
- To explore robotics in Industrial applications

UNIT I INTRODUCTION TO ROBOTICS 9

Robotics -History - Classification and Structure of Robotic Systems - Basic components -Degrees of freedom - Robot joints coordinates- Reference frames - workspace- Robot languages- Robotic sensors- proximity and range sensors, ultrasonic sensor, touch and slip sensor.

UNIT II ROBOT KINEMATICS AND DYNAMICS 9

Kinematic Modelling: Translation and Rotation Representation, Coordinate transformation, DH parameters, Forward and inverse kinematics, Jacobian, Dynamic Modelling: Forward and inverse dynamics, Equations of motion using Euler-Lagrange formulation, Newton Euler formulation.

UNIT III ROBOTICS CONTROL 9

Control of robot manipulator - state equations - constant solutions -linear feedback systems, single-axis PID control - PD gravity control -computed torque control, variable structure control and impedance control.

UNIT IV ROBOT INTELLIGENCE AND TASK PLANNING 9

Artificial Intelligence - techniques - search problem reduction - predicate logic means and end analysis -problem solving -robot learning - task planning - basic problems in task planning - AI in robotics and Knowledge Based Expert System in robotics

UNIT-V INDUSTRIAL ROBOTICS 9

Robot cell design and control - cell layouts - multiple robots and machine interference - work cell design - work cell control - interlocks – error detection deduction and recovery - work cell controller - robot cycle time analysis. Safety in robotics, Applications of robot and future scope.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the end of the course the student will be able to

CO1: Describe the fundamentals of robotics

CO2: Understand the concept of kinematics and dynamics in robotics.

CO3: Discuss the robot control techniques

CO4: Explain the basis of intelligence in robotics and task planning

CO5: Discuss the industrial applications of robotics

REFERENCE:

1. John J. Craig, 'Introduction to Robotics (Mechanics and Control)', Addison-Wesley, 2nd Edition, 2004.
2. Richard D. Klafter, Thomas A. Chmielewski, Michael Negin, 'Robotics Engineering: An Integrated Approach', PHI Learning, New Delhi, 2009.
3. K.S.Fu, R.C.Gonzalez and C.S.G.Lee, 'Robotics Control, Sensing, Vision and Intelligence', Tata McGraw Hill, 2nd Reprint,2008.

4. Reza N.Jazar, 'Theory of Applied Robotics Kinematics, Dynamics and Control', Springer, 1st Indian Reprint, 2010.
5. Mikell. P. Groover, Michell Weis, Roger. N. Nagel, Nicolous G.Odrey, 'Industrial Robotics Technology, Programming and Applications ', McGraw Hill, Int 2012.

VL4092 SOFT COMPUTING AND OPTIMIZATION TECHNIQUES L T P C
3 0 0 3

COURSE OBJECTIVE:

- To classify various soft computing frame works.
- To be familiar with the design of neural networks, fuzzy logic, and fuzzy systems.
- To learn mathematical background for optimized genetic programming.
- Be exposed to neuro-fuzzy hybrid systems and its applications.
- To understand the various evolutionary optimization techniques.

UNIT I FUZZY LOGIC: 9

Introduction to Fuzzy logic - Fuzzy sets and membership functions- Operations on Fuzzy sets- Fuzzy relations, rules, propositions, implications, and inferences- Defuzzification techniques- Fuzzy logic controller design- Some applications of Fuzzy logic.

UNIT II ARTIFICIAL NEURAL NETWORKS: 9

Supervised Learning: Introduction and how brain works, Neuron as a simple computing element, The perceptron, Backpropagation networks: architecture, multilayer perceptron, backpropagation learning-input layer, accelerated learning in multilayer perceptron, The Hopfield network, Bidirectional associative memories (BAM), RBF Neural Network.

Unsupervised Learning: Hebbian Learning, Generalized Hebbian learning algorithm, Competitive learning, Self- Organizing Computational Maps: Kohonen Network.

UNIT III GENETIC ALGORITHM: 9

Genetic algorithm- Introduction - biological background - traditional optimization and search techniques - Genetic basic concepts - operators – Encoding scheme – Fitness evaluation – crossover - mutation - Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.

UNIT IV NEURO-FUZZY MODELING 9

Adaptive Neuro-Fuzzy Inference Systems (ANFIS) – architecture - Coactive Neuro-Fuzzy Modeling, framework, neuron functions for adaptive networks – Data Clustering Algorithms – Rule base Structure Identification –Neuro-Fuzzy Control – the inverted pendulum system.

UNIT V CONVENTIONAL OPTIMIZATION TECHNIQUES 9

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.

TOTAL :45 PERIODS

COURSE OUTCOMES:

Upon Completion of the course, the students will be able to:

CO1: Develop application on different soft computing techniques like Fuzzy, GA and Neural network

CO2: Implement Neuro-Fuzzy and Neuro-Fuzz-GA expert system.
CO3: Implement machine learning through Neural networks.
CO4: Model Neuro Fuzzy system for clustering and classification.
CO5: Able to use the optimization techniques to solve the real world problems

REFERENCES:

1. J.S.R.Jang, C.T. Sun and E.Mizutani, Neuro-Fuzzy and Soft Computing, PHI / Pearson
2. Education 2004.
3. David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009.
4. George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,Prentice Hall, 1995.
5. James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Edn., 2003.
6. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India, 2003.
7. Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 1998.
8. Simon Haykins, Neural Networks: A Comprehensive Foundation, Prentice Hall International Inc, 1999.
9. Timothy J.Ross, Fuzzy Logic with Engineering Applications, McGraw-Hill, 1997.

CU4251	RF SYSTEM DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- Be familiar with RF transceiver system design for wireless communications
- Be exposed to design methods of receivers and transmitters used in communication systems
- Design RF circuits and systems using an advanced design tool.
- Exemplify different synchronization methods circuits and describe their block schematic and design criteria
- Measure RF circuits and systems with a spectrum analyzer.

UNIT I BASICS OF RADIO FREQUENCY SYSTEM DESIGN 9

Definitions and models of Linear systems and Non-linear system. Specification parameters: Gain, noise figure, SNR, Characteristic impedance, S-parameters, Impedance matching and Decibels. Elements of digital base band signalling: complex envelope of band pass signals, Average value, RMS value, Crest factor, Sampling, jitter, modulation techniques, filters, pulse shaping, EVM, BER, sensitivity, selectivity, dynamic range and, adjacent and alternate channel power leakages

UNIT II RADIO ARCHITECTURES AND DESIGN CONSIDERATIONS 9

Superheterodyne architecture, direct conversion architecture, Low IF architecture, band-pass sampling radio architecture, System Design Considerations for an Analog Frontend Receiver in Cognitive Radio Applications, Interference, Near, In-band & wide-band considerations.

UNIT III AMPLIFIER MODELING AND ANALYSIS 9

Noise: Noise equivalent model for Radio frequency device, amplifier noise model, cascade performance, minimum detectable signal, performance of noisy systems in cascade. Non-Linearity: Amplifier power transfer curve, gain compression, AM-AM, AM-PM, polynomial approximations,

Saleh model, Wiener model and Hammerstein model, intermodulation, Single and two tone analyses, second and third order distortions and measurements, SOI and TOI points, cascade performance of nonlinear systems.

UNIT IV MIXER AND OSCILLATOR MODELING AND ANALYSIS 9

Mixers: Frequency translation mechanisms, frequency inversion, image frequencies, spurious calculations, principles of mixer realizations. Oscillators: phase noise and its effects, effects of oscillator spurious components, frequency accuracy, oscillator realizations: Frequency synthesizers, NCO.

UNIT V APPLICATIONS OF SYSTEMS DESIGN 9

Multimode and multiband Superheterodyne transceiver: selection of frequency plan, receiver system and transmitter system design – Direct conversion transceiver: receiver system and transmitter system design.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

Upon the completion of course, students will be able to

CO1: understand the specifications of transceiver modules

CO2: understand pros and cons of transceiver architectures and their associated design considerations

CO3: understand the impact of noise and amplifier non-linearity of amplification modules and also will learn the resultant effect during cascade connections

CO4: get exposure about spurs and generation principles during signal generation and frequency translations

CO5: understand the case study of transceiver systems and aid to select specification parameters

REFERENCES

1. The Design of CMOS Radio-Frequency Integrated Circuits by Thomas H. Lee. Cambridge University Press, 2004.
2. Qizheng Gu, “RF System Design of Transceivers for Wireless Communications”, Springer ,2005.
3. Kevin McClaning, “Wireless Receiver Design for Digital Communications,” Yes Dee Publications, 2012.
4. M C Jeruchim, P Balapan and K S Shanmugam, “Simulation of Communication systems:Modeling, Methodology and Techniques”, Kluwer Academic/Plenum Publishers, 2 nd Edition, 2000.

EL4071 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY L T P C
3 0 0 3

COURSE OBJECTIVES:

- To gain broad conceptual understanding of the various aspects of electromagnetic (EM) interference and compatibility
- To develop a theoretical understanding of electromagnetic shielding effectiveness
- To understand ways of mitigating EMI by using shielding, grounding and filtering
- To understand the need for standards and to appreciate measurement methods
- To understand how EMI impacts wireless and broadband technologies

UNIT I INTRODUCTION & SOURCES OF EM INTERFERENCE 9

Introduction - Classification of sources - Natural sources - Man-made sources - Survey of the electromagnetic environment.

UNIT II EM SHIELDING 9

Introduction - Shielding effectiveness - Far-field sources - Near-field sources - Low-frequency, magnetic field shielding - Effects of apertures

UNIT III INTERFERENCE CONTROL TECHNIQUES 9

Equipment screening - Cable screening - grounding - Power-line filters - Isolation - Balancing - Signal-line filters - Nonlinear protective devices.

UNIT IV EMC STANDARDS, MEASUREMENTS AND TESTING 9

Need for standards - The international framework - Human exposure limits to EM fields -EMC measurement techniques - Measurement tools - Test environments.

UNIT V EMC CONSIDERATIONS IN WIRELESS AND BROADBAND TECHNOLOGIES 9

Efficient use of frequency spectrum - EMC, interoperability and coexistence - Specifications and alliances - Transmission of high-frequency signals over telephone and power networks – EMC and digital subscriber lines - EMC and power line telecommunications.

SUGGESTED ACTIVITIES:

1. Investigate various case studies related to EMIC. Example: Chernobyl Disaster in 1986.
2. Develop some understanding about the design of EM shields in electronic system design and packaging.

COURSE OUTCOMES:

Upon completion of this course, the student will be able to

CO1: Demonstrate knowledge of the various sources of electromagnetic interference
CO2: Display an understanding of the effect of how electromagnetic fields couple through apertures, and solve simple problems based on that understanding
CO3: Explain the EMI mitigation techniques of shielding and grounding
CO4: Explain the need for standards and EMC measurement methods
CO5: Discuss the impact of EMC on wireless and broadband technologies

TOTAL:45 PERIODS

REFERENCES

1. Christopoulos C, Principles and Techniques of Electromagnetic Compatibility, CRC Press, Second Edition, Indian Edition, 2013.

2. Paul C R, Introduction to Electromagnetic Compatibility, Wiley India, Second Edition,2008.
3. Kodali V P, Engineering Electromagnetic Compatibility, Wiley India, Second Edition,2010.
4. Henry W Ott, Electromagnetic Compatibility Engineering, John Wiley & Sons Inc, Newyork,2009.
5. Scott Bennett W, Control and Measurement of Unintentional Electromagnetic Radiation, John Wiley& Sons Inc., Wiley Interscience Series, 1997.

AP4003 VLSI DESIGN TECHNIQUES L T P C
3 0 0 3

COURSE OBJECTIVES:

- To understand the basics I-V characteristics of MOS transistor
- To introduce the VLSI design flow
- To Design combinational and sequential circuits
- To introduce testing of VLSI circuits
- To explore system design using Verilog HDL

Unit I CMOS TECHNOLOGY 9

MOS transistor, Ideal I–V characteristics, C–V characteristics, non-ideal I–V effects – CMOS Inverter and Pass transistor DC transfer characteristics – CMOS technologies, Layout design Rules – Stick Diagram – CMOS process enhancements– VLSI design Flow.

Unit II CIRCUIT DELAY,POWER, INTERCONNECT AND VERILOG HDL 9

Delay estimation – Logical effort and Transistor sizing – Power dissipation – Interconnect – Design margin –Reliability – Scaling – SPICE – Device models.
Verilog: Procedural assignments –conditional statements – Design of combinational and sequential circuits using different types of modeling –Test benches.

Unit III COMBINATIONAL AND SEQUENTIAL CIRCUIT DESIGN 9

Circuit families –Circuit Pitfalls – Sequencing static circuits, Max-min delay constraints, Time borrowing, Clock Skew – circuit design of latches and flip flops – synchronizers, Metastability, communication between asynchronous clock domains.

Unit IV CMOS TESTING 9

Need for testing – Testers, Text fixtures and test programs – Logic verification – Silicon debug principles –Manufacturing test – Design for testability – Boundary scan test.

UNIT V SYSTEM DESIGN USING VERILOG HDL 9

Basic concepts- identifiers- gate primitives- gate delays- operators timing controls- procedural assignments-conditional statements- Design of combinational and sequential circuits using Data flow- structural gate level- switch level modeling and Behavioral modeling-Test benches.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

After the completion of the course the students will be able to,

CO1: Analyze the characteristics of CMOS transistor
CO2: Identify the methods to distribute clock and reduce power dissipation in CMOS circuits.
CO3: Design combinational and sequential circuits
CO4: Analyze the methods to test the CMOS circuits

CO5: Synthesize the combinational and sequential circuits using Verilog HDL

REFERENCES:

1. Weste and Harris: “CMOS VLSI DESIGN” 4th Edition, Pearson Education, 2013
2. Uyemura J.P: “Introduction to VLSI circuits and systems”, Wiley 2002.
3. D.APucknell&K.Eshraghian, “Basic VLSI Design”, 3rd Edition, PHI, 2003
4. Wayne Wolf, “Modern VLSI design”, 4th edition Pearson Education, 2009
5. M.J.S.Smith, “Application specific integrated circuits”, 1st edition, Addison-Wesley Professional,1997
6. Ciletti, “Advanced Digital Design with the Verilog HDL”, 2nd edition, Pearson Education 2010
7. Samir Palnitkar “Verilog HDL a guide to digital design and Synthesis”, Prentice Hall, 2nd edition, 2003

AP4004 NANO TECHNOLOGIES L T P C
3 0 0 3

COURSE OBJECTIVES:

- To introduce the basics of nano electronics
- To understand the basics of semiconductor materials
- To understand the basics of MOSFETS and its application in nano electronics
- To learn the advanced nanoscale devices
- To explore about Biosensors

UNIT I INTRODUCTION TO NANOELECTRONICS 9

Introduction to nanoelectronics, Limitations of conventional microelectronics. Classical Particles, Classical Waves and Quantum Particles-Quantum Mechanics of Electronics -Schrödinger wave equation.

UNIT II MATERIALS FOR NANOELECTRONICS 9

Introduction- Semiconductors, Crystal lattices: Bonding in crystals- Electron energy bands-Semiconductor heterostructures-Lattice-matched and pseudomorphic heterostructures-Carbon nanomaterials: nanotubes and fullerenes.

UNIT III SHRINK-DOWN APPROACHES 9

Moore’s Law- Technology Scaling and Reliability Challenges.Basic MOS Transistor-Types, Modes of operation, n-MOS operation, Drain Current, Threshold Voltage, Energy band diagram of MOSFET, nanoscale MOSFET, SCEs-limits to scaling, system integration limits.

UNIT IV ADVANCED NANOSCALE DEVICES 9

Double Gate MOSFETs, Tri-Gate MOSFETs, Tunnel FETs-Multi-Gate TFETs and Heterojunction TFETs- Graphene and Carbon Nanotube Transistors.

UNIT V FET BASED BIOSENSORS 9

Principles- Components of biosensor-Classification of Biosensors based on transducers, FET based Biosensor- ion-sensitive field effect transistor-operation and fabrication-Characteristics and Performance.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of this course, the students will be able to

CO1: Understand the basic concepts of nano electronics and various aspects of nano electronics. (K2)

CO2: Summarize the basic knowledge of Semiconductor materials and carbon nano tubes. (K2)

CO3: Understand the basic concepts of MOS scaling. (K2)

CO4: understand the advanced nanoscale devices (K3)

CO5: Understand the Bio sensor devices. (K2)

REFERENCES

1. G.W. Hanson, Fundamentals of Nanoelectronics, Pearson, 2009.
2. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, “Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications”, Cambridge University Press 2011.
3. Pierre R. Coulet, Loïc J. Blum, Biosensor Principles and Applications, CRC press-2019.
4. Donald A. Neamen, “Semiconductor Physics and Devices Basic Principles", Third Edition, McGraw-Hill Higher- Education, 2003.

VL4252 VLSI TESTING L T P C

3 0 0 3

COURSE OBJECTIVES:

- to introduce the VLSI testing.
- to introduce logic and fault simulation and testability measures
- to study the test generation for combinational and sequential circuits
- to study the design for testability.
- to study the fault diagnosis

UNIT I INTRODUCTION TO TESTING 9

Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing - Test Economics and Product Quality – Fault Modeling – Relationship Among Fault Models.

UNIT II LOGIC & FAULT SIMULATION & TESTABILITY MEASURES 9

Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – Scoap Controllability and Observability

UNIT III TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG

UNIT IV DESIGN FOR TESTABILITY 9

Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Built-in Self-Test – Random Logic Bist – DFT for Other Test Objectives.

UNIT V FAULT DIAGNOSIS 9

Introduction and Basic Definitions – Fault Models for Diagnosis – Generation of Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Understand VLSI Testing Process
CO2: Develop Logic Simulation and Fault Simulation
CO3: Develop Test for Combinational and Sequential Circuits
CO4: Understand the Design for Testability
CO5: Perform Fault Diagnosis.

REFERENCES

1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, "VLSI Test Principles and Architectures", Elsevier, 2017
2. Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits" , Kluwer Academic Publishers, 2017.
3. Niraj K. Jha and Sandeep Gupta, "Testing of Digital Systems", Cambridge University Press, 2017.

AP4092 EDGE ANALYTICS AND INTERNET OF THINGS L T P C
3 0 0 3

COURSE OBJECTIVES:

- To Understand the basis for intersection of IOT and Edge Analytics
- To Understand the IOT protocols and standards
- To comprehend the use of Machine Learning in Edge Analytics
- To gain understanding on the use of Deep Learning techniques for analytics
- To gain insight into edge analytics models and deployment

UNIT I INTRODUCTION TO IOT 9

Importance and Need for IoT - Application and Use cases of IoT - Overview of Industrial IoT - Intersection of IoT and Edge Analytics.

UNIT II IOT PROTOCOLS AND SYSTEMS 9

IoT protocols and standards - Cloud IoT Infrastructure - Setup and program IoT device- Data Collection from IoT device.

UNIT III MACHINE LEARNING AND ARTIFICIAL INTELLIGENCE 9

Introduction to Machine Learning and Artificial Intelligence - Overview of Deep Learning and Neural Networks- Introduction to Convolution Neural Networks.

UNIT IV AUTO ENCODERS AND ITS PROGRAMMING 9

Introduction to Recurrent Neural Networks- Introduction to Auto Encoders- Programming Practice: Build Image Classifier, Build Anomaly Detector

UNIT V EDGE ANALYTICS **9**

Challenges with Edge Devices and Deployment - Need for Model Quantization Quantization Aware Training- Post Model Quantization- Programming Practice: Model quantization, Deploying model on Edge Devices

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of this course, student will be able to

CO 1: Use the foundational concepts in Edge Analytics for application design and development
CO 2: Use IOT protocols in cloud environments.
CO 3: Implement and use Machine Learning and Artificial Intelligence algorithms and tools
CO 4: implement and use Deep Learning techniques for applications
CO 5: Analyze Edge devices analytics models and and its challenges

REFERENCES:

1. Honbo Zhou, "The Internet of Things in the Cloud: A Middleware Perspective", CRC Press, 2012.
2. P. Flach, "Machine learning: The art and science of algorithms that make sense of datall, Cambridge University Press, 2012.
3. Anirudh Koul, Siddha Ganju, Meher Kasam, "Practical Deep Learning for Cloud, Mobile, and Edge" O'Reilly Media, 2019.
4. Dieter Uckelmann, Mark Harrison, Florian Michahelles, "Architecting the Internet of Things", Springer, 2011.

AP4093 QUANTUM COMPUTING **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To introduce the building blocks of Quantum computers and highlight the paradigm change between conventional computing and quantum computing
- To understand the Quantum state transformations and the algorithms
- To understand entangled quantum subsystems and properties of entangled states
- To explore the applications of quantum computing

UNIT I QUANTUM BUILDING BLOCKS **9**

The Quantum Mechanics of Photon Polarization, Single-Qubit Quantum Systems, Quantum State Spaces, Entangled States, Multiple-Qubit Systems, Measurement of Multiple-Qubit States, EPR Paradox and Bell's Theorem, Bloch sphere

UNIT II QUANTUM STATE TRANSFORMATIONS **9**

Unitary Transformations, Quantum Gates, Unitary Transformations as Quantum Circuits, Reversible Classical Computations to Quantum Computations, Language for Quantum Implementations.

UNIT III QUANTUM ALGORITHMS **9**

Computing with Superpositions, Quantum Subroutines, Quantum Fourier Transformations, Shor's Algorithm and Generalizations, Grover's Algorithm and Generalizations

UNIT IV ENTANGLED SUBSYSTEMS AND ROBUST QUANTUM COMPUTATION 9

Quantum Subsystems, Properties of Entangled States, Quantum Error Correction, Graph states and codes, CSS Codes, Stabilizer Codes, Fault Tolerance and Robust Quantum Computing

UNIT V QUANTUM INFORMATION PROCESSING 9

Limitations of Quantum Computing, Alternatives to the Circuit Model of Quantum Computation, Quantum Protocols, Building Quantum, Computers, Simulating Quantum Systems, Bell states. Quantum teleportation. Quantum Cryptography, no cloning theorem

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the end of the coarse, the student will be able to

CO1: Understand the basic principles of quantum computing.
CO2: Gain knowledge of the fundamental differences between conventional computing and quantum computing.
CO3: Understand several basic quantum computing algorithms.
CO4: Understand the classes of problems that can be expected to be solved well by quantum computers.

CO5: Simulate and analyze the characteristics of Quantum Computing Systems.

REFERENCES:

1. John Gribbin, Computing with Quantum Cats: From Colossus to Qubits, 2021
2. William (Chuck) Easttom, Quantum Computing Fundamentals, 2021
3. Parag Lala, Quantum Computing, 2019
4. Eleanor Rieffel and Wolfgang Polak, QUANTUM COMPUTING A Gentle Introduction, 2011
5. Nielsen M. A., Quantum Computation and Quantum Information, Cambridge University Press.2002
6. Benenti G., Casati G. and Strini G., Principles of Quantum Computation and Information, Vol. I: Basic Concepts, Vol II: Basic Tools and Special Topics, World Scientific. 2004
7. Pittenger A. O., An Introduction to Quantum Computing Algorithms 2000

CU4076 VLSI FOR WIRELESS COMMUNICATION L T P C
3 0 0 3

COURSE OBJECTIVES:

- To understand the concepts of basic wireless communication concepts.
- To study the parameters in receiver and low noise amplifier design.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of transmitters and power amplifiers in wireless communication.

UNIT I COMMUNICATION CONCEPTS 9

Introduction – Overview of Wireless systems – Standards – Access Methods – Modulation schemes – Classical channel – Wireless channel description – Path loss – Multipath fading – Standard Translation.

UNIT II RECEIVER ARCHITECTURE & LOW NOISE AMPLIFIERS 9

Receiver front end – Filter design – Non-idealities – Design parameters – Noise figure & Input intercept point. LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedance matching & Core amplifier.

UNIT III MIXERS 9

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Noise - A Complete Active Mixer. Switching Mixer – Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV FREQUENCY SYNTHESIZERS 9

PLL – Phase detector – Dividers – Voltage Controlled Oscillators – LC oscillators – Ring Oscillators – Phase noise – Loop filters & design approaches – A complete synthesizer design example (DECT) – Frequency synthesizer with fractional divider.

UNIT V TRANSMITTER ARCHITECTURES & POWER AMPLIFIERS 9

Transmitter back end design – Quadrature LO generator – Power amplifier design.

COURSE OUTCOMES:

At the end of this course, the student should be able to

CO1: Able to recollect basic wireless communication concepts.

CO2: To understand the parameters in receiver and design a low noise amplifier

CO3: In a position to apply his knowledge on various types of mixers designed for wireless communication.

CO4: Design PLL and VCO

CO5: Understand the concepts of transmitters and utilize the power amplifiers in wireless communication.

TOTAL : 45 PERIODS

REFERENCES

1. Bosco H Leung “VLSI for Wireless Communication”, Pearson Education, 2002.
2. B.Razavi ,”RF Microelectronics” , Prentice-Hall ,1998.
3. Behzad Razavi, “Design of Analog CMOS Integrated Circuits” McGraw-Hill, 1999.
4. Emad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI wireless design – Circuits & Systems”, Kluwer Academic Publishers, 2000.
5. J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design,” Boston, Kluwer Academic Pub., 1997.
6. Thomas H.Lee, “The Design of CMOS Radio – Frequency Integrated Circuits”, Cambridge University Press ,2003.

AP4005 MICRO ELECTRO MECHANICAL SYSTEMS L T P C
3 0 0 3

COURSE OBJECTIVES:

- To understand the operation of sensors and actuators
- To understand the operation of major classes of MEMS devices/systems
- To give the fundamentals of standard micro fabrication techniques and processes
- To understand the unique demands, environments and applications of MEMS devices
- To understand RF MEMS, Bio MEMS and MOEMS

UNIT I INTRODUCTION TO MEMS 9

Intrinsic Characteristics of MEMS – Energy Domains and Transducers- Sensors and Actuators – Introduction to Micro fabrication - Silicon based MEMS processes – New Materials – Review of Electrical and Mechanical concepts in MEMS – Semiconductor devices – Stress and strain analysis – Flexural beam bending- Torsional deflection.

UNIT II SENSORS AND ACTUATORS 9

Electrostatic sensors – Parallel plate capacitors – Applications – Interdigitated Finger capacitor- Piezoresistive sensors – Piezoresistive sensor materials - piezoelectric effects – piezoelectric materials-Stress analysis of mechanical elements – Thermal Sensing and Actuation – Thermal expansion – Thermal couples – Thermal resistors – Thermal Bimorph - Applications – Magnetic Actuators – Micromagnetic components.

UNIT III MICROMACHINING 9

Silicon Anisotropic Etching – Anisotrophic Wet Etching – Dry Etching of Silicon – Plasma Etching – Deep Reaction Ion Etching (DRIE) – Isotropic Wet Etching – Gas Phase Etchants – Case studies –Basic surface micro machining processes – Structural and Sacrificial Materials – Acceleration of sacrificial Etch – Striction and Antistriction methods – LIGA Process - Assembly of 3D MEMS – Foundry process.

UNIT IV POLYMER AND OPTICAL MEMS 9

Polymers in MEMS – SU-8, PMMA, PDMS, Langmuir – Blodgett Films, Micro System fabrication – Photolithography – Ion implantation- Diffusion – Oxidation – Chemical vapour deposition – Etching- Optical MEMS – Lenses and Mirrors – Actuators for Active Optical MEMS.

UNIT V OVERVIEW OF MEMS AREAS 9

Bonding techniques for MEMS : Surface bonding , Anodic bonding , Silicon - on - Insulator , wire bonding , Sealing – Assembly of micro systems- RF MEMS - switches, active and passive components, Bio MEMS - Microfluidics, Digital Micro fluidics, Ink jet printer,- MOEMS - optical switch, optical cross-connect, tunable VCSEL, micro bolometers.

TOTAL : 45 PERIODS

SUGGESTED ACTIVITIES:

1. Expose the students to occupational environment related to semiconductor devices and MEMS
2. Create opportunity for acquiring practical skills of various field instruments in the area of

MEMS devices

3. Manage the issues arising during the execution of projects related to MEMS.

COURSE OUTCOMES:

At the end of the course the student will be able to:

CO1: Understand the working principles of micro sensors and actuators
CO2: Understand the application of scaling laws in the design of micro systems
CO3: Understand the typical materials used for fabrication of micro machines
CO4: Understand the principles of standard micro fabrication techniques
CO5: Appreciate the challenges in the design and fabrication of RF,Bio, and MOEMS systems

REFERENCES

1. Stephen D Senturia, 'Microsystem Design', Springer Publication, 2000.
2. Chang Liu, 'Foundations of MEMS', Pearson Education Inc., 2012.
3. Marc J. Madou, 'Fundamentals of Microfabrication: The Science of Miniaturization', Second Edition , 2002.
4. Nadim Maluf," An Introduction to Micro Electro Mechanical System Design", Artech House, 2000.
5. Mohamed Gad-el-Hak, editor, " The MEMS Handbook", CRC press Baco Raton, 2001.

AP4006 HARDWARE SECURE COMPUTING L T P C
3 0 0 3

COURSE OBJECTIVES

- Describe the fundamental principles in Data security
- Discuss the watermarking algorithms and its usage
- Explain the physical attacks and Modular arithmetic security methods
- Describe the memory based attacks and vulnerabilities using deceptive mechanisms
- Discuss the methods of FPGA implementation of cryptographic algorithms

UNIT I INTRODUCTION TO CRYPTO ALGORITHMS 9

Cryptography basics, Cryptographic algorithms - Symmetric Key algorithms, Public Key algorithms and Hash Algorithms, Data Encryption Standards, Advanced Encryption Standards, RSA, BowFish .

UNIT II DESIGN INTELLECTUAL PROPERTY PROTECTION 9

Introduction to IP Protection, Watermarking Basics, Watermarking Examples, Good Watermarks, Fingerprinting, Hardware Metering.

UNIT III PHYSICAL ATTACKS AND MODULAR EXPONENTIATION 9

Physical Attacks (PA) Basics, Physical Attacks and Countermeasures, Building Secure Systems, Modular Exponentiation (ME) Basics, ME in Cryptography, ME Implementation and Vulnerability, Montgomery Reduction.

UNIT IV ATTACKS AND COUNTER MEASURES 9

Introduction to Side Channel Attacks, Memory Vulnerabilities and Cache Attacks, Power Analysis, More Attacks and Countermeasures, Modified Modular Exponentiation, Hardware Trojan (HT) and Trusted IC, Hardware Trojan Taxonomy, Hardware Trojan Detection Overview, Hardware Trojan Detection Methods, Trusted IC Design with HT Prevention.

UNIT V EMERGING TECHNOLOGIES 9

FPGA Implementation of Crypto algorithms, Vulnerabilities and Countermeasures in FPGA Systems, Role of Hardware in Security and Trust, Physical Unclonable Functions (PUF) Basics, Reliability, Trust Platform Modules

TOTAL : 45 PERIODS

COURSE OUTCOMES

Upon completion the students will be able to

CO1: Understand the basics of Cryptography(K2)

CO2: Identify the mechanism of Data Integrity protection mechanisms(K2)

CO3: Analyse the counter measures for physical attacks and the use of Modular exponentiation(K2)

CO4: Study side channel attacks and Trojan-based attacks(K2)

CO5: Challenges in Realisation using VLSI implementations(K2)

REFERENCES:

1. Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, Hardware Security: Design, Threats, and Safeguards, CRC Press,2014
2. Tehranipoor, Mohammad, Wang, Introduction to Hardware Security and Trust, Springer,2011.
3. Ted Huffmire, Handbook of FPGA Design Security, Springer,2010.
4. Stefan Mangard, Elisabeth Oswald, Thomas Popp, Power Analysis Attacks - Revealing the Secrets of Smart Cards, Springer,2007.
5. Doug Stinson, Cryptography Theory and Practice, CRC Press,2018.

VL4072 CAD FOR VLSI DESIGN L T P C

3 0 0 3

COURSE OBJECTIVES:

- to introduce the VLSI design methodologies and design methods.
- to introduce data structures and algorithms required for VLSI design.
- to study algorithms for partitioning and placement.
- to study algorithms for floor planning and routing.
- to study algorithms for modelling, simulation and synthesis.

UNIT I INTRODUCTION 9

Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Review of VLSI Design Automation Tools

UNIT II DATA STRUCTURES AND BASIC ALGORITHMS 9

Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.

UNIT III ALGORITHMS FOR PARTITIONING AND PLACEMENT 9

Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction – Partitioning – Placement – Placement Algorithms.

UNIT IV ALGORITHMS FOR FLOORPLANNING AND ROUTING 9

Floorplanning – Problem Formulation – Floorplanning Algorithms – Routing – Area Routing – Global Routing – Detailed Routing.

UNIT V MODELLING, SIMULATION AND SYNTHESIS 9

Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should be able to:

CO1: use various VLSI design methodologies
CO2: understand different data structures and algorithms required for VLSI design.
CO3: develop algorithms for partitioning and placement.
CO4: develop algorithms for floorplanning and routing.
CO5: design algorithms for modelling, simulation and synthesis.

REFERENCES

1. Sabih H. Gerez, “Algorithms for VLSI Design Automation”, Second Edition, Wiley-India, 2017.
2. Naveed a. Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, Springer, 2017.
3. Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, “Handbook of Algorithms for Physical Design Automation, CRC Press, 1st Edition, 2.
4. N.a. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

AP4073 SENSORS AND ACTUATORS L T P C
3 0 0 3

COURSE OBJECTIVES:

- Understand static and dynamic characteristics of measurement systems.
- Study various types of sensors.
- Study different types of actuators and their usage.
- Study State-of-the-art digital and semiconductor sensors.

UNIT I INTRODUCTION TO MEASUREMENT SYSTEMS 9

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance

characteristics: static and dynamic characteristics of measurement systems, zero-order, first-order, and second-order measurement systems and response.

UNIT II RESISTIVE AND REACTIVE SENSORS 9

Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & application to LVDT.

UNIT III SELF-GENERATING SENSORS 9

Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper and low-drift amplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers.

UNIT IV ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS 9

Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.

UNIT V DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS 9

Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, MOSFET transistors, CCD imaging sensors , ultrasonic sensors, fiber-optic sensors.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course the student will be able to :

CO1: Compare Actuators with various drive characteristics.

CO2: Evaluate digital sensors and semiconductor device sensors performance metrics.

CO3: Characterize the performance of Self-generating sensors.

CO4: Analyze the performance of self-generating Sensors.

CO5: Analyze the performance of resistive and reactive sensors.

REFERENCES:

1. Andrzej M. Pawlak Sensors and Actuators in Mechatronics Design and Applications, 2006.
2. D. Johnson, “Process Control Instrumentation Technology”, 8th Ed, 2014, John Wiley and Sons.
3. D.Patranabis, “Sensors and Transducers”, TMH 2003.
4. E.O. Doeblin, “Measurement System: Applications and Design”, McGraw Hill publications,1996
5. Graham Brooker, Introduction to Sensors for ranging and imaging, Yesdee, 2009.
6. Herman K.P. Neubrat, “Instrument Transducers – An Introduction to Their Performance and Design”, Oxford University Press. 22,1999.
7. Ian Sinclair, Sensors and Transducers, Elsevier, 3rd Edition, 2011.

8. Jon Wilson , “Sensor Technology Handbook”, Newne 2004.
9. Kevin James, PC Interfacing and Data acquisition, Elsevier, 2011.
10. Ramon PallásAreny, John G. Webster, “Sensors and Signal conditioning”, 2nd edition, John Wiley and Sons, 2000.
11. Sensors and Actuators: Control System Instrumentation, Clarence W. de Silva CRC Press, 2007

AP4095 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN L T P C
3 0 0 3

COURSE OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the end of the course the student will be able to

CO1: identify sources affecting the speed of digital circuits.

CO2:identify methods to improve the signal transmission characteristics

CO3: characterise and model multiconductor transmission line

CO4: analyse clock distribution system and understand its design parameters
CO5: analyse nonideal effects of transmission line

REFERENCES

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR , 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handboo of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.

TOOLS REQUIRED

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECTRAQUEST from Cadence, http://www.specctraquest.com or any equivalent open source tool

AP4007 CONSUMER ELECTRONICS L T P C
3 0 0 3

COURSE OBJECTIVES:

- To acquaint the students with the construction, theory and operation of the basic electronic devices such as PN junction diode, Bipolar and Field Effect Transistors, Power control devices etc.,
- To know about the working principle of LED, LCD and other Opto-electronic devices.
- To introduce the concept of Sensors and voice controls.
- To provide the knowledge on Smart home devices.
- To gain knowledge on current communication technology.

UNIT I CONSUMER ELECTRONICS FUNDAMENTALS 9

History of Electronic Devices- Vacuum Tubes, Transistors, Integrated Circuits- Moorse Law, Semiconductor Devices, Diodes, Rectifiers, Transistors, Logic Gates, Combinational Circuits, ADC, DAC and Microprocessors, Microprocessor Vs Microcontrollers, Microcontrollers in consumer electronics, Energy management, Intelligent Building Perspective.

UNIT II ENTERTAINMENT ELECTRONICS 9

Audio systems: Construction and working principle of: Microphone, Loud speaker, AM and FM receiver, stereo, Home theatre. Display systems: CRT, LCD, LED and Graphics displays Video Players: DVD and Blue RAY. Recording Systems: Digital Cameras and Camcorders.

UNIT III SMART HOME - SENSORS 9

Technology involved in Smart home, Home Virtual Assistants- Alexa and Google Home. Home Security Systems - Intruder Detection, Automated blinds, Motion Sensors, Thermal Sensors and Image Sensors, PIR, IR and Water Level Sensors.

UNIT IV HOME APPLIANCES 9

Home Enablement Systems: RFID Home, Lighting control, Automatic Cleaning Robots, Washing Machines, Kitchen Electronics- Microwave, Dishwasher, Induction Stoves, Smart Refrigerators, Smart alarms, Smart toilet, Smart floor, Smart locks.

UNIT V INTRODUCTION TO SMART OS AND COMMUNICATION 9

Introduction to Smart OS- Android and iOS. Video Conferencing Systems- Web/IP Camera, Video security, Internet Enabled Systems, Wi-Fi, IoT, Li-Fi, GPS and Tracking Systems. Cordless Telephones, Fax Machines, PDAs- Tablets, Smart Phones and Smart Watches.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon successful completion of this course students will be able to

CO1: Explain the V-I characteristic of diode, UJT and SCR. Describe the equivalence circuits of transistors.

CO2: Operate the basic electronic devices such as PN junction diode, Bipolar and Field Effect Transistors, Power control devices, LED, LCD and other Opto-electronic devices.

CO3: Gain knowledge on sensors and controls.

CO4: Emphasize the need for communication systems.

CO5: Explore the current technology and apply on home applications.

REFERENCES:

1. Thomas L Floyd "Electronic Devices" 10th Edition Pearson Education Asia 2018.
2. Jordan Frith, " Smartphones as Locative Media ", Wiley. 2014.
3. Dennis C Brewer, " Home Automation", Que Publishing 2013.
4. Thomas M. Coughlin, "Digital Storage in Consumer Electronics", Elsevier and Newness 2012.
5. Nick vandome, Smart homes in easy steps, - Master smart technology for your home 2018.

AP4008 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS ARCHITECTURES

L T P C
3 0 0 3

COURSE OBJECTIVES:

- To expose the students to the fundamentals of microprocessor architecture.
- To explore the high performance features in CISC architecture
- To familiarize the high performance features in RISC architecture
- To introduce the basic features in Motorola microcontrollers.
- To enable the students to understand PIC Microcontroller

UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV MSP430 16 - BIT MICROCONTROLLER 9

The MSP430 Architecture- CPU Registers - Instruction Set, On-Chip Peripherals - MSP430 - Development Tools, ADC - PWM - UART - Timer Interrupts - System design using MSP430Microcontroller.

UNIT V PIC MICROCONTROLLER 9

CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter – PWM and introduction to C-Compilers.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course the student will be able to

CO1: To understand the fundamentals of microprocessor architecture.
CO2: To know and appreciate the high performance features in CISC architecture.
CO3: To know and appreciate the high performance features in RISC architecture.
CO4: To perceive the basic features in Motorola microcontrollers.
CO5: To interpret and understand PIC Microcontroller.

REFERENCES:

1. Daniel Tabak , „" Advanced Microprocessors" McGraw Hill.Inc., 1995
2. James L. Antonakos , " The Pentium Microprocessor", Pearson Education , 1997.
3. Steve Furber , " ARM System –On –Chip architecture", Addision Wesley , 2000.
4. Gene .H.Miller ." Micro Computer Engineering ", Pearson Education , 2003.
5. John .B.Peatman , " Design with PIC Microcontroller" , Prentice hall, 1997.
6. John H.Davis , "MSP 430 Micro controller basics", Eelsevier, 2008.
7. James L.Antonakos, "An Introduction to the Intel family of Microprocessors", Pearson Education 1999.
8. Barry.B.Breg, "The Intel Microprocessors Architecture , Programming and Interfacing ", PHI,2002.
9. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001.
10. Readings: Web links -- www.ocw.mit.edu, www.arm.com

AP4009 BIOMEDICAL SIGNAL PROCESSING L T P C

3 0 0 3

COURSE OBJECTIVES:

- Describe the properties and suitable models of biomedical signals
- Introduce the basic signal processing techniques in analyzing biomedical signals
- Develop computational skills in filtering of biomedical signals
- Develop an understanding on ECG signal compression algorithms
- Develop an understanding on feature extraction of biomedical signals

UNIT I INTRODUCTION TO BIOMEDICAL SIGNALS 9

Introduction to Biomedical Signals: The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives and difficulties in Biomedical analysis. Electrocardiography: Basic electrocardiography, ECG lead systems, ECG signal characteristics. Signal Conversion :Simple signal conversion systems, Conversion requirements for biomedical signals, Signal conversion circuits

UNIT II SIGNAL AVERAGING 9

Signal Averaging: Basics of signal averaging, signal averaging as a digital filter, a typical averager, software for signal averaging, limitations of signal averaging. Adaptive Noise Cancelling: Principal noise canceller model, 60-Hz adaptive cancelling using a sine wave model, other applications of adaptive filtering

UNIT III DATA COMPRESSION TECHNIQUES 9

Data Compression Techniques: Turning point algorithm, AZTEC algorithm, Fan algorithm, Huffman coding, data reduction algorithms The Fourier transform, Correlation, Convolution, Power spectrum estimation, Frequency domain analysis of the ECG

UNIT IV CARDIOLOGICAL SIGNAL PROCESSING 9

Cardiological signal processing: Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Realtime ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor

UNIT V NEUROLOGICAL SIGNAL PROCESSING 9

Neurological signal processing: The brain and its potentials, The electrophysiological origin of brain waves, The EEG signal and its characteristics (EEG rhythms, waves, and transients), Correlation. Analysis of EEG channels: Detection of EEG rhythms, Template matching for EEG, spike and wave detection

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the end of this course the student will be able to

CO1: Possess skills necessary to analyze ECG and EEG Signals

CO2: Apply classical and modern filtering techniques for ECG and EEG Signals

CO3: Apply classical and modern compression techniques for ECG and EEG Signals

CO4: Develop an understanding on ECG feature extraction

CO5: Develop an understanding on EEG feature extraction

REFERENCES

1. Rangaraj M Rangayyan “Biomedical Signal Analysis – A case study approach” IEEE press series in biomedical engineering, First Edition, 2002

2. John G Proakis, Dimitris and G. Manolakis, “Digital Signal Processing Principles algorithms, applications” PHI Third Edition. 2006

3. Willis J. Tompkins " Biomedical Digital Signal Processing", EEE, PHI, 2004

4. D C Reddy "Biomedical Signal Processing: Principles and Techniques", Tata McGraw-Hill Publishing Co. Ltd, 2005

5. J G Webster "Medical Instrumentation: Application & Design", John Wiley & Sons Inc., 2001

AP4010 MODELING AND SYNTHESIS WITH HDL L T P C
3 0 2 4

COURSE OBJECTIVES:

- To know the basic language features of Verilog HDL and its the role in digital logic design.
- To know the behavioural modeling of combinational and sequential circuits.
- To know the behavioural modeling of algorithmic state machines.
- To know the synthesis of combinational and sequential descriptions.
- To know the architectural features of programmable logic devices.

UNIT I INTRODUCTION TO LOGIC DESIGN WITH VERILOG 07

Overview of Digital Design with Verilog HDL - Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block - **Basic Concept- Modules and Ports**: Module definition, port declaration, connecting ports, hierarchical name referencing. **Tasks and Functions**

UNIT II LEVELS OF MODELING 12

Gate-Level Modeling : Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. **Dataflow Modeling:** Continuous assignments, delay specification, expressions, operators, operands, operator types. **Behavioral Modeling:** Structured procedures, initial and always, blocking and nonblocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.

UNIT III DESIGN OF DIGITAL LOGIC USING HDL 12

Design of combinational logic: adders, multiplexers, de-multiplexers,encoders and decoders,comparators,multipliers - **Design of Sequential logic** : Flip-flops, synchronous and Asynchronous counters, shift registers, Universal shift register,FSM and LFSR.
(Using various Levels of Modeling)

UNIT IV LOGIC SYNTHESIS AND DESIGN FLOW 07

Logic Synthesis with verilog HDL-Synthesis Design flow, RTL and Test Bench Modeling Techniques and Timing and Path Delay Modeling, Timing Checks, Switch Level Modeling

UNIT V PROGRAMMABLE LOGIC DEVICES 07

Programmable logic devices, storage devices, programmable logic array programmable array logic, programmability of PLDs CPLDs.

45 PERIODS

PRACTICAL EXERCISES: **30 PERIODS**

1. Design Entry Using VHDL Or Verilog Using HDL Languages of
   I. Combinational Circuits Namely 8:1 Mux/Demux, Full Adder, 8-Bit Magnitude Comparator, Encoder/Decoder, Priority Encoder.
   Ii. Sequential Circuits Namely D-FF, 4-Bit Shift Registers (SISO, SIPO, PISO, Bidirectional), 3-Bit Synchronous Counters.
2. Test Vector Generation And Timing Analysis of Sequential And Combinational Logic Design for exercise (1) above.
   2. Synthesis, P&R and Post P&R Simulation of the Components Simulated In (1) Above.
3. FPGA Implementation of PCI Bus & Arbiter. .
   Verifying Design Functionality Using Either Chipscope Feature (Xilinx) /the Signal Tap Feature (Altera)/Other Equivalent Feature . Invoke the PLL And Demonstrate the Use of the PLL Module for Clock Generation in FPGAs.

COURSE OUTCOMES:

After successful completion of the course, the students are able to

CO1: demonstrate knowledge on HDL design flow and digital circuits design.

CO2:design and develop the combinational and sequential circuits using various modeling

CO3:solving algorithmic state machines using hardware description language

CO4:analyze the process of synthesizing the combinational and sequential descriptions

CO5:know the advantages of programmable logic devices and their description in Verilog

TOTAL : 45 +30=75 PERIODS

REFERENCES

1. Samir Palnitkar - Verilog HDL, 2nd edition, Pearson Education, 2003.
2. Michael D Ciletti - Advanced Digital Design with the VERILOG HDL, 2ND Edition, PHI, 2009.
3. Z Navabi - Verilog Digital System Design, 2nd Edition, McGraw Hill, 2005.
4. Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with Verilog, 2nd Edition, TMH, 2008.

IF4071 **DEEP LEARNING** **L T P C**
3 0 2 4

COURSE OBJECTIVES:

- Develop and Train Deep Neural Networks.
- Develop a CNN, R-CNN, Fast R-CNN, Faster-R-CNN, Mask-RCNN for detection and recognition
- Build and train RNNs, work with NLP and Word Embeddings
- The internal structure of LSTM and GRU and the differences between them
- The Auto Encoders for Image Processing

UNIT I DEEP LEARNING CONCEPTS **6**

Fundamentals about Deep Learning. Perception Learning Algorithms. Probabilistic modelling. Early Neural Networks. How Deep Learning different from Machine Learning. Scalars. Vectors. Matrixes, Higher Dimensional Tensors. Manipulating Tensors. Vector Data. Time Series Data. Image Data.

Video Data.

UNIT II NEURAL NETWORKS 9

About Neural Network. Building Blocks of Neural Network. Optimizers. Activation Functions. Loss Functions. Data Pre-processing for neural networks, Feature Engineering. Overfitting and Underfitting. Hyperparameters.

UNIT III CONVOLUTIONAL NEURAL NETWORK 10

About CNN. Linear Time Invariant. Image Processing Filtering. Building a convolutional neural network. Input Layers, Convolution Layers. Pooling Layers. Dense Layers. Backpropagation Through the Convolutional Layer. Filters and Feature Maps. Backpropagation Through the Pooling Layers. Dropout Layers and Regularization. Batch Normalization. Various Activation Functions. Various Optimizers. LeNet, AlexNet, VGG16, ResNet. Transfer Learning with Image Data. Transfer Learning using Inception Oxford VGG Model, Google Inception Model, Microsoft ResNet Model. R-CNN, Fast R-CNN, Faster R-CNN, Mask-RCNN, YOLO

UNIT VI NATURAL LANGUAGE PROCESSING USING RNN 10

About NLP & its Toolkits. Language Modeling . Vector Space Model (VSM). Continuous Bag of Words (CBOW). Skip-Gram Model for Word Embedding. Part of Speech (PoS) Global Co-occurrence Statistics–based Word Vectors. Transfer Learning. Word2Vec. Global Vectors for Word Representation GloVe. Backpropagation Through Time. Bidirectional RNNs (BRNN) . Long Short Term Memory (LSTM). Bi-directional LSTM. Sequence-to-Sequence Models (Seq2Seq). Gated recurrent unit GRU.

UNIT V DEEP REINFORCEMENT & UNSUPERVISED LEARNING 10

About Deep Reinforcement Learning. Q-Learning. Deep Q-Network (DQN). Policy Gradient Methods. Actor-Critic Algorithm. About Autoencoding. Convolutional Auto Encoding. Variational Auto Encoding. Generative Adversarial Networks. Autoencoders for Feature Extraction. Auto Encoders for Classification. Denoising Autoencoders. Sparse Autoencoders

LIST OF EXPERIMENTS: 30

1: Feature Selection from Video and Image Data
2: Image and video recognition
3: Image Colorization
4: Aspect Oriented Topic Detection & Sentiment Analysis
5: Object Detection using Autoencoder

COURSE OUTCOMES:

CO1: Feature Extraction from Image and Video Data
CO2: Implement Image Segmentation and Instance Segmentation in Images
CO3: Implement image recognition and image classification using a pretrained network (Transfer Learning)
CO4: Traffic Information analysis using Twitter Data
CO5: Autoencoder for Classification & Feature Extraction

TOTAL : 45+30=75 PERIODS

REFERENCES

1. Deep Learning A Practitioner's Approach Josh Patterson and Adam Gibson O'Reilly Media, Inc.2017

2. Learn Keras for Deep Neural Networks, Jojo Moolayil, Apress,2018
3. Deep Learning Projects Using TensorFlow 2, Vinita Silaparasetty, Apress, 2020
4. Deep Learning with Python, FRANÇOIS CHOLLET, MANNING SHELTER ISLAND,2017
5. Pro Deep Learning with TensorFlow, Santanu Pattanayak, Apress,2017

AP4011 ADVANCED DIGITAL IMAGE PROCESSING L T P C
3 0 2 4

COURSE OBJECTIVES:

- To understand the image fundamentals and mathematical transforms necessary for image processing and to study the image enhancement techniques.
- To understand the image segmentation and representation techniques.
- To understand how image are analyzed to extract features of interest.
- To introduce the concepts of image registration and image fusion.
- To analyze the constraints in image processing when dealing with 3D data sets.

UNIT I FUNDAMENTALS OF DIGITAL IMAGE PROCESSING 9

Elements of visual perception, brightness, contrast, hue, saturation, mach band effect, 2D image transforms-DFT, DCT, KLT, and SVD. Image enhancement in spatial and frequency domain, Morphological image processing.

UNIT II SEGMENTATION 9

Edge detection, Thresholding, Region growing, Fuzzy clustering, Watershed algorithm, Active contour methods, Texture feature-based segmentation, Model based segmentation, Atlas based segmentation, Wavelet based Segmentation methods.

UNIT III FEATURE EXTRACTION 9

First and second order edge detection operators, Phase congruency, Localized feature extraction-detecting image curvature, shape features Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Run length features, Fractal model-based features, Gabor filter, wavelet features.

UNIT IV REGISTRATION AND IMAGE FUSION 9

Registration- Pre-processing, Feature selection-points, lines, regions and templates Feature Correspondence-Point pattern matching, Line matching, region matching Template matching. Transformation functions-Similarity transformation and Affine Transformation. Resampling- Nearest Neighbour and Cubic Splines Image Fusion-Overview of image fusion, pixel fusion, Multiresolution based fusion discrete wavelet transforms, Curvelet transform. Region based fusion.

UNIT V 3D IMAGE VISUALIZATION 9

Sources of 3D Data sets, Slicing the Data set, Arbitrary section planes, The use of color, Volumetric display, Stereo Viewing, Ray tracing, Reflection, Surfaces, multiply connected surfaces, Image processing in 3D, Measurements on 3D images.

PRACTICALS:

1. Wavelet and DCT based Image Compression
2. Geometrical transformations and Interpolation of Images
3. Edge Detection using Canny edge detector
4. Region based , threshold based and Watershed Segmentation
5. Image filtering using DFT
6. Texture, Gabor and Wavelet Feature Extraction
7. Image fusion using Wavelets
8. Segmenting 3D Image volume using K-means clustering.
9. Segmentation of Lungs from 3D- Chest Scan.

COURSE OUTCOMES:

Upon Completion of the course, the students will be able to

CO1: To understand image formation and the role of human visual system plays in perception of gray and color image data.

CO2: To apply image processing techniques in both the spatial and frequency (Fourier) domains.

CO3: To design image analysis techniques in the form of image segmentation and to evaluate the methodologies for segmentation.

CO4: To conduct independent study and analysis of feature extraction techniques.

CO5: To understand the concepts of image registration and image fusion.

CO6: To analyze the constraints in image processing when dealing with 3D data sets and to apply image processing algorithms in practical applications.

TOTAL: 45+30=75 PERIODS

REFERENCES

1. John C.Russ, “The Image Processing Handbook”, CRC Press, 2007.
2. Mark Nixon, Alberto Aguado, “Feature Extraction and Image Processing”, Academic Press, 2008.
3. Ardeshir Goshtasby, “2D and 3D Image registration for Medical, Remote Sensing and Industrial Applications”, John Wiley and Sons, 2005.
4. Rafael C. Gonzalez, Richard E. Woods, , Digital Image Processing', Pearson, Education, Inc., Second Edition, 2004.
5. Anil K. Jain, , Fundamentals of Digital Image Processing', Pearson Education, Inc., 2002.
6. Rick S.Blum, Zheng Liu,“ Multisensor image fusion and its Applications“, Taylor & Francis, 2006.

AP4072 **PCB DESIGN** **L T P C**

3 0 2 4

COURSE OBJECTIVES:

- Understand the need for PCB Design and steps involved in PCB Design and Fabrication process.
- Familiarize Schematic and layout design flow using Electronic Design Automation (EDA)

Tools.

- Understand basic concepts of transmission line, crosstalk and thermal issues
- Design (schematic and layout) PCB for analog circuits, digital circuits and mixed circuits.
- Schematic creation & interpretation

UNIT I INTRODUCTION TO PRINTED CIRCUIT BOARD 9

Introduction to Printed circuit board: fundamental of electronic components, basic electronic circuits, Basics of printed circuit board designing: Layout planning, general rules and parameters, ground conductor considerations, thermal issues, check and inspection of artwork.

UNIT II DESIGN RULES FOR PCB 9

Design rules for PCB: Design rules for Digital circuit PCBs, Analog circuit PCBs, high frequency and fast pulse applications, Power electronic applications, Microwave applications,
PCB Technology Trends: Multilayer PCBs. Multiwire PCB, Flexible PCBs, Surface mount PCBs, Reflow soldering, Introduction to High-Density Interconnection (HDI) Technology.

UNIT III INTRODUCTION TO ELECTRONIC DESIGN AUTOMATION(EDA) TOOLS FOR PCB DESIGNING 9

Introduction to Electronic design automation(EDA) tools for PCB designing: Brief Introduction of various simulators,SPICE and PSPICE Environment, Selecting the Components Footprints as per design, Making New Footprints, Assigning Footprint to components, Net listing, PCB Layout Designing, Auto routing and manual routing. Assigning specific text (silkscreen) to design, Creating report of design, creating manufacturing data (GERBER) for design.

UNIT IV INTRODUCTION PRINTED CIRCUIT BOARD PRODUCTION TECHNIQUES 9

Introduction printed circuit board production techniques: Photo printing, film-master production, reprographic camera, basic process for double sided PCBs photo resists, Screen printing process, plating, relative performance and quality control, Etching machines, Solders alloys, fluxes, soldering techniques, Mechanical operations

UNIT V PCB DESIGN FOR EMI/EMC 9

PCB design for EMI/EMC: Subsystem/PCB Placement in an enclosure, Filtering circuit placement, decoupling and bypassing, Electronic discharge protection, Electronic waste; Printed circuit boards Recycling techniques, Introduction to Integrated Circuit Packaging and footprints, NEMA and IPC standards.

SUGGESTED ACTIVITIES:

1. Using any Electronic design automation (EDA) software, Practice following PCB Design steps (Open source EDA Tool KiCad Preferable or equivalent) Example circuit: Basic RC Circuit Schematic Design: Familiarization of the Schematic Editor, Schematic creation, Annotation, Netlist generation Layout Design: Familiarization of Footprint Editor, Mapping of components, Creation of PCB layout Schematic Create new schematic components Create new component footprints.
2. Fabricate single-sided PCB, mount the components and assemble in a cabinet for any one of the circuits mentioned below.

3. Regulator circuit using 7805.
4. Astable or Monostable multivibrator using IC555
5. RC Phase-shift or Wein-bridge Oscillator using transistor.
6. 4 bit binary /MOD N counter using D-Flip flops.
7. Design a 8051 Development board having Power section consisting of IC7805, capacitor, resistor, headers, LED,Serial communication section consisting of MAX 232, Capacitors,DB9 connector, Jumper, LEDs, Reset & Input/ output sections consisting of89C51 Microcontroller, Electrolytic Capacitor, Resistor, Jumper, Crystal Oscillator, Capacitors.
8. Touch plate switches – transistorized or 555 based
9. Doorbell/cordless bell
10. Clapping switch and IR switch
11. Blinkers
12. Cell charger, battery charger, mobile charger
13. Fire/smoke/intruder alarm
14. Liquid level controller
15. Audio amplifiers

COURSE OUTCOMES:

Upon the completion of this course, students will demonstrate the ability to:

CO1: Appreciate the necessity and evolution of PCB, types and classes of PCB.

CO2: Understand the steps involved in schematic, layout, fabrication and assembly process of PCB design.

CO3: Apply advanced techniques, skills and modern tools for designing and fabrication of PCBs.

CO4: Apply the knowledge and techniques to fabricate Multilayer, SMT and HDI PCB.

CO5: Design (schematic and layout) and fabricate PCB for simple circuits.

TOTAL : 45+30=75 PERIODS

REFERENCES

1. Printed circuit board design ,fabrication assembly and testing By R. S. Khandpur, Tata McGraw Hill 2006

2. Printed Circuits Handbook, Sixth Edition,by Clyde F. Coombs, Jr, Happy T. Holden,Publisher: McGraw-Hill Education Year: 2016

3. Complete PCB Design Using OrCAD Capture and PCB Editor,Kraig Mitzner Bob Doe Alexander Akulin Anton Suponin Dirk Müller, 2nd Edition 2009.

4. Introduction to System-on-Package, Rao R ,Tummala,&MadhavanSwaminathan, McGraw Hill, 2008

5. EMC and Printed circuit board ,Design theory and layout, Mark I Montrose IEEE compatibility society

6. Electronic Product Design Volume-I by S D Mehta, S Chand Publications

7. Open source EDA Tool KiCad Tutorial: http://kicad-pcb.org/help/tutorials/

8. PCB Fabrication user guide page: http://www.wikihow.com/Create-Printed-Circuit-Boards , http://www.siongboon.com/projects/2005-09-07_home_pcb_fabrication/ ,
9. http://reprap.org/wiki/MakePCBInstructions#Making_PCBs_yourself

10. PCB Fabrication at home(video): https://www.youtube.com/watch?v=mv7Y0A9YeUc,
11. https://www.youtube.com/watch?v=imQTCW1yWkg

AUDIT COURSES

AX4091 ENGLISH FOR RESEARCH PAPER WRITING L T P C
2 0 0 0

COURSE OBJECTIVES:

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

UNIT I INTRODUCTION TO RESEARCH PAPER WRITING 6

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II PRESENTATION SKILLS 6

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III TITLE WRITING SKILLS 6

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV RESULT WRITING SKILLS 6

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V VERIFICATION SKILLS 6

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission

TOTAL: 30 PERIODS

COURSE OUTCOMES:

CO1 –Understand that how to improve your writing skills and level of readability
CO2 – Learn about what to write in each section
CO3 – Understand the skills needed when writing a Title
CO4 – Understand the skills needed when writing the Conclusion
CO5 – Ensure the good quality of paper at very first-time submission

REFERENCES:

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006

3. Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
4. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.

AX4092 DISASTER MANAGEMENT L T P C
2 0 0 0

COURSE OBJECTIVES:

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT I INTRODUCTION 6

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II REPERCUSSIONS OF DISASTERS AND HAZARDS 6

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III DISASTER PRONE AREAS IN INDIA 6

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT IV DISASTER PREPAREDNESS AND MANAGEMENT 6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V RISK ASSESSMENT 6

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival

TOTAL : 30 PERIODS

COURSE OUTCOMES:

CO1: Ability to summarize basics of disaster

CO2: Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.

CO3: Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

CO4: Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
CO5: Ability to develop the strengths and weaknesses of disaster management approaches

REFERENCES:

1. Goel S. L., Disaster Administration And Management Text And Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2. NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company,2007.
3. Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences And Reflections", Prentice Hall OfIndia, New Delhi,2001.

AX4093 CONSTITUTION OF INDIA L T P C
2 0 0 0

COURSE OBJECTIVES:

Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.

UNIT I HISTORY OF MAKING OF THE INDIAN CONSTITUTION

History, Drafting Committee, (Composition & Working)

UNIT II PHILOSOPHY OF THE INDIAN CONSTITUTION

Preamble, Salient Features

UNIT III CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES

Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT IV ORGANS OF GOVERNANCE

Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V LOCAL ADMINISTRATION

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy(Different departments), Village level:Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT VI ELECTION COMMISSION

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization
- of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

SUGGESTED READING

1. The Constitution of India,1950(Bare Act),Government Publication.
2. Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,1st Edition, 2015.
3. M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

AX4094 **நற்றமிழ் இலக்கியம்** **L T P C**
2 0 0 0

UNIT I **சங்க இலக்கியம்** **6**

1. தமிழின் துவக்க நூல் தொல்காப்பியம்
   – எழுத்து, சொல், பொருள்
2. அகநானூறு (82)
   - இயற்கை இன்னிசை அரங்கம்
3. குறிஞ்சிப் பாட்டின் மலர்க்காட்சி
4. புறநானூறு (95,195)
   - போரை நிறுத்திய ஔவையார்

UNIT II **அறநெறித் தமிழ்** **6**

1. அறநெறி வகுத்த திருவள்ளுவர்
   - அறம் வலியுறுத்தல், அன்புடைமை, ஒப்புறவு அறிதல், ஈகை, புகழ்
2. பிற அறநூல்கள் - இலக்கிய மருந்து
   – ஏலாதி, சிறுபஞ்சமூலம், திரிகடுகம், ஆசாரக்கோவை (தூய்மையை வலியுறுத்தும் நூல்)

UNIT III **இரட்டைக் காப்பியங்கள்** **6**

1. கண்ணகியின் புரட்சி

- சிலப்பதிகார வழக்குரை காதை

2. சமூகசேவை இலக்கியம் மணிமேகலை
   - சிறைக்கோட்டம் அறக்கோட்டமாகிய காதை

UNIT IV **அருள்நெறித் தமிழ்** **6**

1. சிறுபாணாற்றுப்படை
   - பாரி முல்லைக்குத் தேர் கொடுத்தது, பேகன் மயிலுக்குப் போர்வை கொடுத்தது, அதியமான் ஔவைக்கு நெல்லிக்கனி கொடுத்தது, அரசர் பண்புகள்
2. நற்றிணை
   - அன்னைக்குரிய புன்னை சிறப்பு
3. திருமந்திரம் (617, 618)
   - இயமம் நியமம் விதிகள்
4. தர்மச்சாலையை நிறுவிய வள்ளலார்
5. புறநானூறு
   - சிறுவனே வள்ளலானான்
6. அகநானூறு (4) - வண்டு
   நற்றிணை (11) - நண்டு
   கலித்தொகை (11) - யானை, புறா
   ஐந்திணை 50 (27) - மான்

ஆகியவை பற்றிய செய்திகள்

UNIT V **நவீன தமிழ் இலக்கியம்** **6**

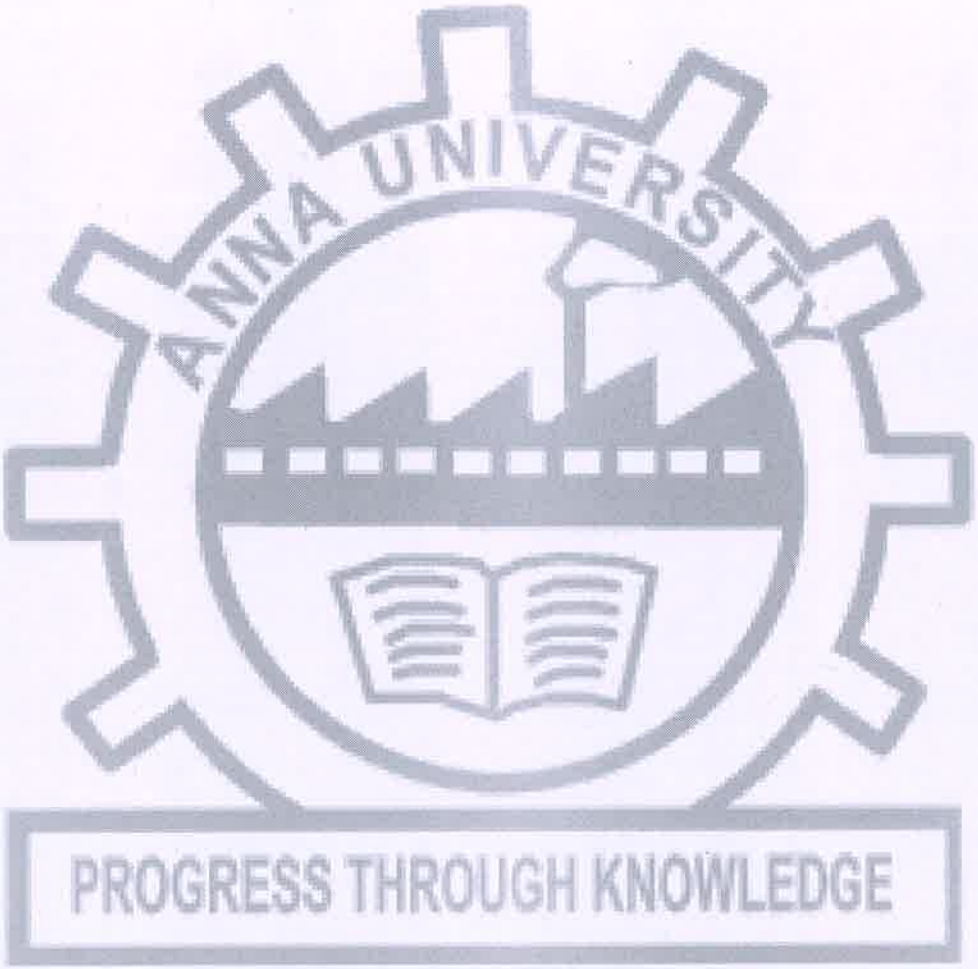
1. உரைநடைத் தமிழ்,
   - தமிழின் முதல் புதினம்,
   - தமிழின் முதல் சிறுகதை,
   - கட்டுரை இலக்கியம்,
   - பயண இலக்கியம்,
   - நாடகம்,
2. நாட்டு விடுதலை போராட்டமும் தமிழ் இலக்கியமும்,
3. சமுதாய விடுதலையும் தமிழ் இலக்கியமும்,
4. பெண் விடுதலையும் விளிம்பு நிலையினரின் மேம்பாட்டில் தமிழ் இலக்கியமும்,
5. அறிவியல் தமிழ்,
6. இணையத்தில் தமிழ்,
7. சுற்றுச்சூழல் மேம்பாட்டில் தமிழ் இலக்கியம்.

TOTAL: 30 PERIODS

<u>தமிழ் இலக்கிய வெளியீடுகள் / புத்தகங்கள்</u>

1. தமிழ் இணைய கல்விக்கழகம் (Tamil Virtual University)- www.tamilvu.org
2. தமிழ் விக்கிப்பீடியா (Tamil Wikipedia) -https://ta.wikipedia.org

3. தர்மபுர ஆதீன வெளியீடு
4. வாழ்வியல் களஞ்சியம்
   - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்
5. தமிழ்கலைக் களஞ்சியம்
   - தமிழ் வளர்ச்சித் துறை (thamilvalarchithurai.com)
6. அறிவியல் களஞ்சியம்
   - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்



PRINCIPAL
JKK MUNIRAJAH COLLEGE
OF TECHNOLOGY
T.N. PALAYAM (Po)-638 506.
GOBI (Tk), ERODE (Dt).

ANNA UNIVERSITY, CHENNAI
AFFILIATED INSTITUTIONS
M.E.APPLIED ELECTRONICS
REGULATIONS – 2017
CHOICE BASED CREDIT SYSTEM

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

1. To enable graduates to develop solutions to real world problems in the frontier areas of Applied Electronics.
2. To enable the graduates to adapt to the latest trends in technology through self-learning and to pursue research to meet out the demands in industries and Academia.
3. To enable the graduates to exhibit leadership skills and enhance their abilities through lifelong learning.

PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAMME SPECIFIC OUTCOMES (PSOs)

PSO1: To critically evaluate the design and provide optimal solutions to problem areas in advanced signal processing, digital system design, embedded systems and VLSI design.

PSO2: **To e**nhance and develop electronic systems using modern engineering hardware and software tools.

PSO3: To work professionally and ethically in applied electronics and related areas.

Mapping of Programme Educational Objectives (PEOs) and the Program Outcomes (Pos):

PEOs	PROGRAM OUTCOMES (POS)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
PEO1	3	3	3	2	2	1	1	-	2	3	2	2
PEO2	3	2	2	2	2	-	-	2	3	3	3	3
PEO3	3	2	2	2	2	1	1	3	2	3	2	3

Mapping of Programme Specific Outcomes (PSOs) and the Program Outcomes (Pos):

PSOs	PROGRAM OUTCOMES (POS)											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
PSO1	3	3	3	2	2	1	1	1	2	3	2	2
PSO2	3	2	3	2	3	-	-	2	3	3	2	2
PSO3	3	2	2	2	-	3	1	3	2	3	2	3

M.E. APPLIED ELECTRONICS
SEMESTER COURSE WISE PO MAPPING

		SUBJECTS	PROGRAMME OUTCOMES											
			PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
I YEAR	SEMESTER I	Applied Mathematics for Electronics Engineers	3	3	2	1				3	2	3		2
		Advanced Digital System Design	3	2	2	2	1			3	2	3		2
		Advanced Digital Signal Processing	3	2	2	2	1			3	2	3		2
		Embedded System Design	3	2	2	2	2			3	2	3		2
		Sensors, Actuators and Interface Electronics	3	2	2	1				3	2	3		2
		Professional Elective I												
		Digital Control Engineering	3	2	2	1				3	2	3		2
		Computer Architecture and Parallel Processing	3	2	2	1				3	2	3		2
		CAD for VLSI	3	2	2	2	1			3	2	3		2
		Electromagnetic Interference and Compatibility	3	2	2	1				3	2	3		2
		Electronic System Design Lab I	3	2	2	2	2			3	3	3		2
	SEMESTER II	Soft Computing and Optimization Techniques	3	2	2	2	1			3	2	3		2
		ASIC and FPGA Design	3	2	2	2				3	2	3		2
		Hardware – Software Co-design	3	2	2	2				3	2	3		2
		Digital Image Processing	3	2	2	2	1			3	2	3		2
		Professional Elective - II												
		VLSI Design Techniques	3	2	2	2	1			3	2	3		2

		Nano Electronics	3	2	1					3	2	3		2
		Wireless Adhoc and Sensor Networks	3	2	1					3	2	3		2
		High Performance Networks	3	2	1					3	2	3		2
		Professional Elective - III												
		DSP Architectures and Programming	3	2	2	2	2			3	2	3		2
		RF System Design	3	2	2	1				3	2	3		2
		Speech and Audio Signal Processing	3	2	2	1	1			3	2	3		2
		Solid State Device Modeling and Simulation	3	2	2	1				3	2	3		2
		Electronic System Design Lab II	3	2	2	2	2			3	3	3		2
		Term Paper Writing and Seminar	3	2	2	1				3	3	3		3
II YEAR	**SEMESTER III**	Advanced Microprocessors and Microcontrollers Architectures	3	2	2	2				3	2	3		2
		Professional Elective –IV												
		Internet of Things	3	2	2	2	1			3	2	3		2
		System on Chip Design	3	2	2	1	1			3	2	3		2
		Robotics	3	2	2	2	1			3	2	3		2
		Physical Design of VLSI Circuits	3	2	2	1				3	2	3		2
		Professional Elective V												
		Signal Integrity for High Speed Design	3	2	1					3	2	3		2
		MEMS and NEMS	3	2	1					3	2	3		2
		Secure Computing Systems	3	2	2	1				3	2	3		2
		Pattern Recognition	3	2	2					3	2	3		2
		Project Work Phase I	3	3	3	3	3	2	2	3	3	3	3	3
	SEM IV	Project Work Phase – II	3	3	3	3	3	2	2	3	3	3	3	3

ANNA UNIVERSITY, CHENNAI
AFFILIATED INSTITUTIONS
M.E. APPLIED ELECTRONICS
REGULATIONS – 2017
CHOICE BASED CREDIT SYSTEM
CURRICULA AND SYLLABI

SEMESTER I

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	MA5152	Applied Mathematics for Electronics Engineers	FC	4	4	0	0	4
2.	AP5151	Advanced Digital System Design	PC	3	3	0	0	3
3.	AP5152	Advanced Digital Signal Processing	PC	5	3	2	0	4
4.	AP5191	Embedded System Design	PC	3	3	0	0	3
5.	AP5101	Sensors, Actuators and Interface Electronics	PC	3	3	0	0	3
6.		Professional Elective I	PC	3	3	0	0	3
PRACTICALS								
7.	AP5111	Electronic System Design Laboratory I	PC	4	0	0	4	2
			TOTAL	**25**	**19**	**2**	**4**	**22**

SEMESTER II

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	AP5251	Soft Computing and Optimization Techniques	PC	3	3	0	0	3
2.	AP5252	ASIC and FPGA Design	PC	3	3	0	0	3
3.	AP5291	Hardware – Software Co-design	PC	3	3	0	0	3
4.	AP5292	Digital Image Processing	PC	3	3	0	0	3
5.		Professional Elective II	PE	3	3	0	0	3
6.		Professional Elective III	PE	3	3	0	0	3
PRACTICALS								
7.	AP5211	Electronic System Design Laboratory II	PC	4	0	0	4	2
8.	CP5281	Term Paper Writing and Seminar	EEC	2	0	0	2	1
			TOTAL	**24**	**18**	**0**	**6**	**21**

SEMESTER III

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
THEORY								
1.	AP5301	Advanced Microprocessors and Microcontrollers Architectures	PC	3	3	0	0	3
2.		Professional Elective IV	PE	3	3	0	0	3
3.		Professional Elective V	PE	3	3	0	0	3
PRACTICALS								
4.	AP5311	Project Work Phase I	EEC	12	0	0	12	6
			TOTAL	**21**	**9**	**0**	**12**	**15**

SEMESTER IV

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
PRACTICALS								
1.	AP5411	Project Work Phase II	EEC	24	0	0	24	12
				TOTAL	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS: 70

FOUNDATION COURSES (FC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	MA5152	Applied Mathematics for Electronics Engineers	FC	4	4	0	0	4

PROFESSIONAL CORE (PC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	AP5151	Advanced Digital System Design	PC	3	3	0	0	3
2.	AP5152	Advanced Digital Signal Processing	PC	5	3	2	0	4
3.	AP5191	Embedded System Design	PC	3	3	0	0	3
4.	AP5101	Sensors, Actuators and Interface Electronics	PC	3	3	0	0	3
5.	AP5111	Electronic System Design Lab I	PC	4	0	0	4	2
6.	AP5251	Soft Computing and Optimization Techniques	PC	3	3	0	0	3
7.	AP5252	ASIC and FPGA Design	PC	3	3	0	0	3
8.	AP5291	Hardware – Software Co-design	PC	3	3	0	0	3
9.	AP5292	Digital Image Processing	PC	3	3	0	0	3
10.	AP5211	Electronic System Design Lab II	PC	4	0	0	4	2
11.	AP5301	Advanced Microprocessor and Microcontroller Architecture	PC	3	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSE (EEC)

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	CP5281	Term Paper Writing and Seminar	EEC	2	0	0	2	1
2.	AP5311	Project Work Phase – I	EEC	12	0	0	12	6
3.	AP5411	Project Work Phase – II	EEC	24	0	0	24	12

PROFESSIONAL ELECTIVES (PE)*

SEMESTER I

ELECTIVE I

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	AP5091	Digital Control Engineering	PE	3	3	0	0	3
2.	AP5001	Computer Architecture and Parallel Processing	PE	3	3	0	0	3
3.	AP5002	CAD for VLSI Circuits	PE	3	3	0	0	3
4.	CU5292	Electromagnetic Interference and Compatibility	PE	3	3	0	0	3

SEMESTER II

ELECTIVE II

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	AP5003	VLSI Design Techniques	PE	3	3	0	0	3
2.	AP5071	Nano Electronics	PE	3	3	0	0	3
3.	CU5097	Wireless Adhoc and Sensor Networks	PE	3	3	0	0	3
4.	AP5004	High Performance Networks	PE	3	3	0	0	3

SEMESTER II

ELECTIVE III

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	DS5191	DSP Processor Architecture and Programming	PE	3	3	0	0	3
2.	AP5073	RF System Design	PE	3	3	0	0	3
3.	AP5074	Speech and Audio Signal Processing	PE	3	3	0	0	3
4.	AP5092	Solid State Device Modeling and Simulation	PE	3	3	0	0	3

SEMESTER III
ELECTIVE IV

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	CP5292	Internet of Things	PE	3	3	0	0	3
2.	AP5005	System on Chip Design	PE	3	3	0	0	3
3.	AP5093	Robotics	PE	3	3	0	0	3
4.	AP5006	Physical Design of VLSI Circuits	PE	3	3	0	0	3

SEMESTER III
ELECTIVE V

SL. NO	COURSE CODE	COURSE TITLE	CATEGORY	CONTACT PERIODS	L	T	P	C
1.	AP5094	Signal Integrity for High Speed Design	PE	3	3	0	0	3
2.	VL5091	MEMS and NEMS	PE	3	3	0	0	3
3.	AP5007	Secure Computing Systems	PE	3	3	0	0	3
4.	AP5008	Pattern Recognition	PE	3	3	0	0	3

MA5152 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS L T P C
4 0 0 4

OBJECTIVES:

The main objective of this course is to demonstrate various analytical skills in applied mathematics and extensive experience with the tactics of problem solving and logical thinking applicable in electronics engineering. This course also will help the students to identify, formulate, abstract, and solve problems in electrical engineering using mathematical tools from a variety of mathematical areas, including fuzzy logic, matrix theory, probability, dynamic programming and queuing theory.

UNIT I FUZZY LOGIC 12

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II MATRIX THEORY 12

Cholesky decomposition - Generalized Eigenvectors - Canonical basis - QR factorization - Least squares method - Singular value decomposition.

UNIT III PROBABILITY AND RANDOM VARIABLES 12

Probability – Axioms of probability – Conditional probability – Baye's theorem - Random variables - Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random variable.

UNIT IV DYNAMIC PROGRAMMING 12

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V QUEUEING MODELS 12

Poisson Process – Markovian queues – Single and multi server models – Little's formula - Machine interference model – Steady state analysis – Self service queue.

TOTAL: 60 PERIODS

OUTCOMES:

After completing this course, students should demonstrate competency in the following skills:

- Concepts of fuzzy sets, knowledge representation using fuzzy rules, fuzzy logic, fuzzy prepositions and fuzzy quantifiers and applications of fuzzy logic.
- Apply various methods in matrix theory to solve system of linear equations.
- Computation of probability and moments, standard distributions of discrete and continuous random variables and functions of a random variable.
- Conceptualize the principle of optimality and sub-optimization, formulation and computational procedure of dynamic programming
- Exposing the basic characteristic features of a queuing system and acquire skills in analyzing queuing models.
- Using discrete time Markov chains to model computer systems.

REFERENCES:

1. Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011.
2. George, J. Klir. and Yuan, B., "Fuzzy sets and Fuzzy logic, Theory and Applications", Prentice Hall of India Pvt. Ltd., 1997.
3. Gross, D., Shortle J. F., Thompson, J.M., and Harris, C. M., "Fundamentals of Queueing Theory", 4th Edition, John Wiley, 2014.
4. Johnson, R.A., Miller, I and Freund J., "Miller and Freund's Probability and Statistics for Engineers", Pearson Education, Asia, 8th Edition, 2015.
5. Taha, H.A., "Operations Research: An Introduction", 9th Edition, Pearson Education, Asia, New Delhi, 2016.

AP5151 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To introduce methods to analyze and design synchronous and asynchronous sequential circuits.
- To introduce the architectures of programmable devices.
- To introduce design and implementation of digital circuits using programming tools.

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Analyze and design sequential digital circuits
- Identify the requirements and specifications of the system required for a given application
- Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:

1. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001
5. Parag K.Lala “Digital system Design using PLD” B S Publications,2003
6. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
7. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

AP5152	ADVANCED DIGITAL SIGNAL PROCESSING	L	T	P	C
		3	2	0	4

OBJECTIVES:

- The student comprehends mathematical description and modelling of discrete time random signals.
- The student is conversant with important theorems and random signal processing algorithms.
- The student learns relevant figures of merit such as power, energy, bias and consistency.
- The student is familiar with estimation, prediction, filtering, multirate concepts and techniques.

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9+6

Discrete random processes – Ensemble averages – Wide sense stationary process – Properties - Ergodic process – Sample mean & variance - Auto-correlation and Auto-correlation matrices- Properties – White noise process – Weiner Khitchine relation - Power spectral density – Filtering random process – Spectral Factorization Theorem – Special types of Random Processes – AR,MA, ARMA Processes – Yule-Walker equations.

UNIT II SPECTRUM ESTIMATION 9+6

Bias and Consistency of estimators - Non-Parametric methods – Periodogram – Modified Periodogram – Barlett's method – Welch's mehod – Blackman-Tukey method – Parametric methods – AR, MA and ARMA spectrum estimation - Performance analysis of estimators.

UNIT III SIGNAL MODELING AND OPTIMUM FILTERS 9+6

Introduction- Least square method – Pade approximation – Prony's method – Levinson Recursion – Lattice filter - FIR Wiener filter – Filtering – Linear Prediction – Non Causal and Causal IIR Weiner Filter -– Mean square error – Discrete Kalman filter.

UNIT IV ADAPTIVE FILTERS 9+6

FIR Adaptive filters - Newton's steepest descent method – Widrow Hoff LMS Adaptive algorithm – Convergence – Normalized LMS – Applications – Noise cancellation - channel equalization – echo canceller – Adaptive Recursive Filters - RLS adaptive algorithm – Exponentially weighted RLS-sliding window RLS.

UNIT V MULTIRATE SIGNAL PROCESSING 9+6

Decimation - Interpolation – Sampling Rate conversion by a rational factor I/D – Multistage implementation of sampling rate conversion – Polyphase filter structures – Applications of multirate signal processing.

TOTAL45+30: 75 PERIODS

OUTCOMES:

- Formulate time domain and frequency domain description of Wide Sense Stationary process in terms of matrix algebra and relate to linear algebra concepts.
- State W-K theorem, spectral factorization theorem, spectrum estimation, bias and consistency of estimators.
- Wiener filtering, LMS algorithms, Levinson recursion algorithm, applications of adaptive filters
- Decimation, interpolation, Sampling rate conversion, Applications of multirate signal processing

REFERENCES:

1. John G. Proakis, Dimitris G. Manolakis, “Digital Signal Processing”, Prentice Hall of India, New Delhi, 2005.
2. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley and Sons Inc., New York, 2006.
3. P. P. Vaidyanathan, “Multirate Systems and Filter Banks”, Prentice Hall, 1992.
4. S. Kay,” Modern spectrum Estimation theory and application”, Prentice Hall, Englehood Cliffs, NJ1988.
5. Simon Haykin, “Adaptive Filter Theory”, Prentice Hall, Englehood Cliffs, NJ1986.
6. Sophoncles J. Orfanidis, “Optimum Signal Processing “, McGraw-Hill, 2000.

AP5191 EMBEDDED SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

The students should be made to:

- Learn design challenges and design methodologies
- Study general and single purpose processor
- Understand bus structures

UNIT I EMBEDDED SYSTEM OVERVIEW 9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR 9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer’s view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES 9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I^2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11**.**

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS 9

Basic State Machine Model, Finite-State Machine with Datapath Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

UNIT V EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS 9

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Explain different protocols
- Discuss state machine and design process models
- Outline embedded software development tools and RTOS

REFERENCES:

1. Bruce Powel Douglas, “Real time UML, second edition: Developing efficient objects for embedded systems”, 3rd Edition 1999, Pearson Education.
2. Daniel W. Lewis, “Fundamentals of embedded software where C and assembly meet”, Pearson Education, 2002.
3. Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & sons, 2002.
4. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.

AP5101 SENSORS, ACTUATORS AND INTERFACE ELECTRONICS L T P C
3 0 0 3

OBJECTIVES:

- Understand static and dynamic characteristics of measurement systems.
- Study various types of sensors.
- Study different types of actuators and their usage.
- Study State-of-the-art digital and semiconductor sensors.

UNIT I INTRODUCTION TO MEASUREMENT SYSTEMS 9

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance characteristics: static characteristics of measurement systems, accuracy, precision, sensitivity, other characteristics: linearity, resolution, systematic errors, random errors, dynamic characteristics of measurement systems: zero-order, first-order, and second-order measurement systems and response.

UNIT II RESISTIVE AND REACTIVE SENSORS 9

Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & application to the LVDT.

UNIT III SELF-GENERATING SENSORS 9

Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper and low-drift amplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers.

UNIT IV ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS 9

Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.

UNIT V DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS 9

Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, saw sensors, digital flow meters, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on MOSFET transistors, CCD imaging sensors , ultrasonic sensors, fiber-optic sensors.

TOTAL: 45 PERIODS

OUTCOMES:

Upon completion of the course the student will be able to

- Compare Actuators
- Evaluate digital sensors and semiconductor device sensors
- Discuss Self-generating sensors

REFERENCES:

1. Andrzej M. Pawlak Sensors and Actuators in Mechatronics Design and Applications, 2006.
2. D. Johnson, “Process Control Instrumentation Technology”, John Wiley and Sons.
3. D.Patranabis, “Sensors and Transducers”, TMH 2003.
4. E.O. Doeblin, “Measurement System : Applications and Design”, McGraw Hill publications
5. Graham Brooker, Introduction to Sensors for ranging and imaging, Yesdee, 2009.
6. Herman K.P. Neubrat, “Instrument Transducers – An Introduction to Their Performance and Design”, Oxford University Press. 22.
7. Ian Sinclair, Sensors and Transducers, Elsevier, 3rd Edition, 2011.
8. Jon Wilson , “Sensor Technology Handbook”, Newne 2004.
9. Kevin James, PC Interfacing and Data acquisition, Elsevier, 2011.
10. Ramon PallásAreny, John G. Webster, “Sensors and Signal Conditioning”, 2nd edition, John Wiley and Sons, 2000.
11. Sensors and Actuators: Control System Instrumentation, Clarence W. de Silva CRC Press , 2007.

AP5111 ELECTRONICS SYSTEM DESIGN LABORATORY I L T P C

0 0 4 2

OBJECTIVES:

- To study of different interfaces
- To learn asynchronous and clocked synchronous sequential circuits
- To understand the concept of built in self test and fault diagnosis

1. System design using PIC, MSP430, ‘51 Microcontroller and 16- bit Microprocessor - 8086.
2. Study of different interfaces (using embedded microcontroller)
3. Implementation of Adaptive Filters and multistage multirate system in DSP Processor
4. Simulation of QMF using Simulation Packages
5. Analysis of Asynchronous and clocked synchronous sequential circuits

6. Built in self test and fault diagnosis
7. Sensor design using simulation tools
8. Design and analysis of real time signal processing system – Data acquisition and signal processing

TOTAL: 60 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to:

- Apply PIC, MSP430, '51 Microcontroller and 8086 for system design
- Simulate QMF
- Design sensor using simulation tools
- Design and analyze of real time signal processing system

AP5251	SOFT COMPUTING AND OPTIMIZATION TECHNIQUES	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn various Soft computing frameworks.
- To familiarizes with the design of various neural networks.
- To understand the concept of fuzzy logic.
- To gain insight onto Neuro Fuzzy modeling and control.
- To gain knowledge in conventional optimization techniques.
- To understand the various evolutionary optimization techniques.

UNIT I NEURAL NETWORKS 9

Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map , Adaptive Resonance Architectures, Hopfield network

UNIT II FUZZY LOGIC 9

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making

UNIT III NEURO-FUZZY MODELING 9

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification – Neuro-Fuzzy Control – Case Studies.

UNIT IV CONVENTIONAL OPTIMIZATION TECHNIQUES 9

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.

UNIT V EVOLUTIONARY OPTIMIZATION TECHNIQUES 9

Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.

TOTAL :45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to:

- Implement machine learning through Neural networks.
- Develop a Fuzzy expert system.
- Model Neuro Fuzzy system for clustering and classification.
- Able to use the optimization techniques to solve the real world problems

REFERENCES :

1. David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009.
2. George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,Prentice Hall, 1995.
3. James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Edn., 2003.
4. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India, 2003.
5. Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 1998.
6. Simon Haykins, Neural Networks: A Comprehensive Foundation, Prentice Hall International Inc, 1999.
7. Singiresu S. Rao, Engineering optimization Theory and practice, John Wiley & sons, inc,Fourth Edition, 2009
8. Timothy J.Ross, Fuzzy Logic with Engineering Applications, McGraw-Hill, 1997.
9. Venkata Rao, Vimal J. Savsani, Mechanical Design Optimization Using Advanced Optimization Techniques, springer 2012

AP5252 ASIC AND FPGA DESIGN L T P C

3 0 0 3

OBJECTIVES:

- To study the design flow of different types of ASIC.
- To familiarize the different types of programming technologies and logic devices.
- To learn the architecture of different types of FPGA.
- To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC

UNIT I OVERVIEW OF ASIC AND PLD 9

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

UNIT II ASIC PHYSICAL DESIGN 9

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction - DRC

UNIT III LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT IV FIELD PROGRAMMABLE GATE ARRAYS 9

FPGA Design : FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

UNIT V SOC DESIGN 9

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies: Canonical Signed Digit Arithmetic, Knowledge Crunching Machine, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

TOTAL: 45 PERIODS

OUTCOMES:

- To analyze the synthesis, Simulation and testing of systems.
- To apply different high performance algorithms in ASICs.
- To discuss the design issues of SOC.

REFERENCES:

1. David A.Hodges, Analysis and Design of Digital Integrated Circuits (3/e), MGH 2004
2. H.Gerez, Algorithms for VLSI Design Automation, John Wiley, 1999
3. Jan. M. Rabaey et al, Digital Integrated Circuit Design Perspective (2/e), PHI 2003
4. M.J.S. Smith : Application Specific Integrated Circuits, Pearson, 2003
5. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
6. P.K.Chan& S. Mourad, Digital Design using Field Programmable Gate Array, Prentice Hall.
7. Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier, 2008
8. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Pub.
9. S.Brown,R.Francis, J.Rose, Z.Vransic, Field Programmable GateArray, Kluwer Pub. 5. Richard FJinder , “Engineering Digital Design,”Academic press

AP5291 HARDWARE - SOFTWARE CO-DESIGN L T P C

3 0 0 3

OBJECTIVES:

- To acquire the knowledge about system specification and modelling.
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation.

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II HARDWARE / SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms .

UNIT III HARDWARE / SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping ,Target Architecture- ArchitectureSpecialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification ,Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co- simulation.

TOTAL:45 PERIODS

OUTCOMES:

- To assess prototyping and emulation techniques
- To compare hardware / software co-synthesis.
- To formulate the design specification and validate its functionality by simulation

REFERENCES:

1. Giovanni De Micheli , Rolf Ernst Morgon," Reading in Hardware/Software Co-Design "Kaufmann Publishers,2001.
2. Jorgen Staunstrup, Wayne Wolf ,"Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub,1997.
3. Ralf Niemann , "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 1998.

AP5292 DIGITAL IMAGE PROCESSING L T P C

3 0 0 3

OBJECTIVES:

The students should be made to:

- Understand fundamentals of digital images
- Learn different image transforms
- Study concept of segmentation

UNITI DIGITAL IMAGE FUNDAMENTALS 9

A simple image model, Sampling and Quantization, Imaging Geometry, Digital Geometry, Image Acquisition Systems, Different types of digital images. Basic concepts of digital distances, distance transform, medial axis transform, component labeling, thinning, morphological processing, extension to gray scale morphology.

UNIT II IMAGE TRANSFORMS 9

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III SEGMENTATION OF GRAY LEVEL IMAGES 9

Histogram of gray level images, multilevel thresholding, Optimal thresholding using Bayesian classification, Watershed and Dam Construction algorithms for segmenting gray level image. Detection of edges and lines: First order and second order edge operators, multi-scale edge detection, Canny's edge detection algorithm, Hough transform for detecting lines and curves, edge linking.

UNIT IV IMAGE ENHANCEMENT AND COLOR IMAGE PROCESSING 9

Point processing, Spatial Filtering, Frequency domain filtering, multi-spectral image enhancement, image restoration. Color Representation, Laws of color matching, chromaticity diagram, color enhancement, color image segmentation, color edge detection, color demosaicing.

UNIT V IMAGE COMPRESSION 9

Lossy and lossless compression schemes, prediction based compression schemes, vector quantization, sub-band encoding schemes, JPEG compression standard, Fractal compression scheme, Wavelet compression scheme.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Discuss image enhancement techniques
- Explain color image processing
- Compare image compression schemes

REFERENCES:

1. A.K. Jain, “Fundamentals of Digital Image Processing”, Prentice-Hall, Addison-Wesley, 1989.
2. B. Jähne, “Practical Handbook on Image Processing for Scientific Applications“, CRC Press,1997.
3. Bernd Jähne, Digital Image Processing, Springer-Verlag Berlin Heidelberg 2005.
4. Bovik (ed.), “Handbook of Image and Video Processing”, Academic Press, 2000.
5. Gonzalez and Woods, Digital Image Processing, Prentice-Hall.
6. J. C. Russ. The Image Processing Handbook. CRC, Boca Raton, FL, 4th edn., 2002.
7. J. S. Lim, “Two-dimensional Signal and Image Processing” Prentice-Hall, 1990.
8. M. Petrou, P. Bosdogianni, “Image Processing, The Fundamentals“, Wiley, 1999.
9. Rudra Pratap, Getting Started With MATLAB 7. Oxford University Press, 2006
10. Stephane Marchand-Maillet, Yazid M. Sharaiha, Binary Digital Image Processing, A Discrete Approach, Academic Press, 2000.
11. W. K. Pratt. Digital image processing, PIKS Inside. Wiley, New York, 3rd, edn., 2001.

AP5211 ELECTRONICS SYSTEM DESIGN LABORATORY II L T P C

0 0 4 2

OBJECTIVES:

- To study of 32 bit ARM7 microcontroller RTOS and its application
- To understand testing RTOS environment and system programming
- To learn wireless network design using embedded systems
- To learn System design using ASIC
- To know use of Verilog and VHDL in sequential digital system modeling

1. Study of 32 bit ARM7 microcontroller RTOS and its application
2. Testing RTOS environment and system programming
3. Designing of wireless network using embedded systems
4. Implementation of ARM with FPGA
5. Design and Implementation of ALU in FPGA using VHDL and Verilog
6. Modeling of Sequential Digital system using Verilog and VHDL
7. Flash controller programming - data flash with erase, verify and fusing
8. System design using ASIC
9. Design, simulation and analysis of signal integrity

TOTAL: 60 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Utilize ARM with FPGA
- Demonstrate design of ALU in FPGA using VHDL and Verilog
- Assess flash controller programming - data flash with erase, verify and fusing
- Explain design, simulation and analysis of signal integrity

CP5281 TERM PAPER WRITING AND SEMINAR L T P C
0 0 2 1

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (atleast 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing each paper.
6. Preparing a working outline
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.
Activities to be carried Out

Activity	Instructions	Submission week	Evaluation
Selection of area of interest and Topic	You are requested to select an area of interest, topic and state an objective	2nd week	**3 %** Based on clarity of thought, current relevance and clarity in writing
Stating an Objective			

Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society 2. List 2 journals 3. List 2 conferences, symposia or workshops 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularly in your area 7. Attach a call for papers (CFP) from your area.	3rd week	**3%** (the selected information must be area specific and of international and national standard)
Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter	• You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar • When picking papers to read - try to: • Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, • Favour papers from well-known journals and conferences, • Favour "first" or "foundational" papers in the field (as indicated in other people's survey paper), • Favour more recent papers, • Pick a recent survey of the field so you can quickly gain an overview, • Find relationships with respect to each other and to your topic area (classification scheme/categorization) • Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered.	4th week	**6%** (the list of standard papers and reason for selection)
Reading and notes for first 5 papers	Reading Paper Process • For each paper form a Table answering the following questions: • What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • How does the work build on other's work, in the author's opinion? • What simplifying assumptions does the author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and	5th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

	compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)		
Reading and notes for next5 papers	Repeat Reading Paper Process	6th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for final 5 papers	Repeat Reading Paper Process	7th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	**8%**(this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	**6%** (Clarity, purpose and conclusion) **6%** Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	**5%** (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11thweek	**10%** (this component will be evaluated based on the linking and classification among the papers)
Your conclusions	Write your conclusions and future work	12th week	**5%** (conclusions – clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th week	**10%** (formatting, English, Clarity and linking) **4%** Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th & 15th week	**10%** (based on presentation and Viva-voce)

TOTAL : 30 PERIODS

AP5301	ADVANCED MICROPROCESSORS AND MICROCONTROLLERS ARCHITECTURES	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To familiarize about the features, specification and features of modern microprocessors.
- To gain knowledge about the architecture of Intel 32 and 64 bit microprocessors and salient features associated with them.
- To familiarize about the features, specification and features of modern microcontrollers.
- To gain knowledge about the 32 bit microcontrollers based on ARM and PIC32 architectures

UNIT I FEATURES OF MODERN MICROPROCESSORS 9

Evolution of microprocessors - Data and Address buses – clock speed – memory interface - multi-core architectures – cache memory hierarchy – operating modes – super scaler execution – dynamic execution – over clocking – integrated graphics processing - performance benchmarks.

UNIT I HIGH PERFORMANCE CISC ARCHITECTURES 9

Introduction to IA 32 bit architecture – Intel Pentium Processors family tree – Memory Management – Branch prediction logic - Superscalar architecture – Hyper threading technology – 64 bit extension technology – Intel 64 bit architecture - Intel Core processor family tree – Turbo boost technology – Smart cache - features of Nehalem microarchitecture

UNIT II HIGH PERFORMANCE RISC ARCHITECTURE - ARM 9

RISC architecture merits and demerits – The programmer's model of ARM Architecture – 3-stage pipeline ARM organization - 3-stage pipeline ARM organization – ARM instruction execution – Salient features of ARM instruction set - ARM architecture profiles (A, R and M profiles)

UNIT III FEATURES OF MODERN MICROPROCESSORS 9

Introduction to microcontrollers – microcontroller vs microprocessors – microcontroller architecture - Processor Core – Memory interfaces– Communication interfaces (SPI,I^2C, USB and CAN) – ADC - PWM – Watchdog timers – Interrupts – Debugging interfaces

UNIT IV HIGH PERFORMANCE MICROCONTROLLER ARCHITECTURES 9

Introduction to the Cortex-M Processor Family - ARM 'Cortex-M3' architecture for microcontrollers – Thumb 2 instruction technology – Internal Registers - Nested Vectored Interrupt controller - Memory map - Interrupts and exception handling – Applications of Cotex-M3 architecture

TOTAL : 45 PERIODS

OUTCOMES:

After completion of the course, the students should be able

- To explain the features and important specifications of modern microprocessors
- To explain the salient features CISC microprocessors based on IA-32 bit and IA-64 bit architectures
- To explain the salient features RISC processors based on ARM architecture and different application profiles of ARM core
- To explain the features and important specifications of modern microcontrollers
- To explain about ARM – M3 architecture and its salient features

REFERENCES:

1. Barry. B. Breg," The Intel Microprocessors" , PHI,2008.
2. Gene .H.Miller ." Micro Computer Engineering ," Pearson Education , 2003.
3. Intel Inc, "Intel 64 and IA-32 Architectures Developer's Manual", Volume-I, 2016
4. Joseph Yiu, "The Definitive Guide to the ARM ® Cortex-M3", Newnes, 2010.
5. Scott Mueller, "Upgrading and Repairing PCs", 20th edition, Que.
6. Steve Furber, '' ARM System –On –Chip architecture "Addision Wesley , 2000.
7. Trevor Martin, "The Designer's Guide to the Cortex-M Processor Family", Newnes, 2013.

AP5091 DIGITAL CONTROL ENGINEERING L T P C
3 0 0 3

OBJECTIVES:

- The student learns the principles of PI,PD,PID controllers.
- The student analyses time and frequency response discrete time control system.
- The student is familiar with digital control algorithms.
- The student has the knowledge to implement PID control algorithms.

UNIT I CONTROLLERS IN FEEDBACK SYSTEMS 9

Review of frequency and time response analysis and specifications of first order and second order feedback control systems, need for controllers, continuous time compensations, continuous time PI, PD, PID controllers, digital PID controllers.

UNIT II BASIC DIGITAL SIGNAL PROCESSING IN CONTROL SYSTEMS 9

Sampling theorem, quantization, aliasing and quantization error, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING OF SAMPLED DATA CONTROL SYSTEM 9

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state space description, first companion, second companion, Jordan canonical models, discrete state variable models (elementary principles only).

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS 9

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS 9

Algorithm development of PID control algorithms, standard programmes for microcontroller implementation, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems, DSP implementation of motor control system.

TOTAL: 45 PERIODS

OUTCOMES:

- Describe continuous time and discrete time controllers analytically.
- Define and state basic analog to digital and digital to analog conversion principles.
- Analyze sampled data control system in time and frequency domains.
- Design simple PI, PD, PID continuous and digital controllers.
- Develop schemes for practical implementation of temperature and motor control systems.

REFERENCES:

1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill,1995.
2. Kenneth J. Ayala, "The 8051 Microcontroller- Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.
3. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.

AP5001 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- Understand the difference between pipeline and parallel processing concepts
- Study various types of processor architectures and the importance of scalable architectures
- Study Memory Architectures, Memory Technology and Optimization.

UNIT I COMPUTER DESIGN AND PERFORMANCE MEASURES 9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors –Multi-vector and SIMD architectures – Multithreaded architectures – Stanford Dash multiprocessor – KSR1 - Data-flow architectures - Performance Measures

UNIT II PARALLEL PROCESSING, PIPELINING AND ILP 9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Pipelining processors - Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors

UNIT III MEMORY HIERARCHY DESIGN 9

Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.

UNIT IV MULTIPROCESSORS 9

Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

UNIT V MULTI-CORE ARCHITECTURES 9

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case-studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture – hp architecture.

TOTAL : 45 PERIODS

OUTCOMES:

- Explain design of memory hierarchies
- Assess Performance Issues and Synchronization issues
- Compare multicore architectures

REFERENCES:

1. David E. Culler, Jaswinder Pal Singh, “Parallel Computing Architecture: A hardware/ software approach”, Morgan Kaufmann / Elsevier, 1997
2. Dimitrios Soudris, Axel Jantsch, "Scalable Multi-core Architectures: Design Methodologies and Tools", Springer, 2012
3. Hwang Briggs, “Computer Architecture and parallel processing”, McGraw Hill, 1984.
4. John L. Hennessey and David A. Patterson, “Computer Architecture – A quantitative approach”, Morgan Kaufmann / Elsevier, 4th. edition, 2007
5. John P. Hayes, “Computer Architecture and Organization”, McGraw Hill
6. John P. Shen, “Modern processor design. Fundamentals of super scalar processors”, Tata McGraw Hill 2003
7. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001
8. William Stallings, “Computer Organization and Architecture – Designing for Performance”, Pearson Education, Seventh Edition, 2006

AP5002 CAD FOR VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To study various physical design methods in VLSI.
- To understand the concepts behind the VLSI design rules and routing techniques.
- To understand the concepts of various algorithms used for floor planning and routing techniques.

UNIT I INTRODUCTION TO VLSI DESIGN FLOW 9

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT II LAYOUT, PLACEMENT AND PARTITIONING 9

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

UNIT III FLOOR PLANNING AND ROUTING 9

Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

UNIT IV SIMULATION AND LOGIC SYNTHESIS 9

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS 9

Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

TOTAL: 45 PERIODS

OUTCOMES:

- To use the simulation techniques at various levels in VLSI design flow
- Discuss the concepts of floor planning and routing
- Outline high level synthesis

REFERENCES:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
3. Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”, World scientific 1999.
4. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing 1987.

CU5292 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY L T P C
3 0 0 3

OBJECTIVES:

The students should be made to be familiar with:

- The basics of EMI
- EMI sources.
- EMI problems.
- Solution methods in PCB.
- Measurements techniques for emission.
- Measurement techniques for immunity.

UNIT I BASIC THEORY 9

Introduction to EMI and EMC, Intra and inter system EMI, Elements of Interference, Sources and Victims of EMI, Conducted and Radiated EMI emission and susceptibility, Case Histories, Radiation hazards to humans, Various issues of EMC, EMC Testing categories EMC Engineering Application.

UNIT II COUPLING MECHANISM 9

Electromagnetic field sources and Coupling paths, Coupling via the supply network, Common mode coupling, Differential mode coupling, Impedance coupling, Inductive and Capacitive coupling, Radioactive coupling, Ground loop coupling, Cable related emissions and coupling, Transient sources, Automotive transients.

UNIT III EMI MITIGATION TECHNIQUES 9

Working principle of Shielding and Murphy"s Law, LF Magnetic shielding, Apertures and shielding effectiveness, Choice of Materials for H, E, and free space fields, Gasketting and sealing, PCB Level shielding, Principle of Grounding, Isolated grounds, Grounding strategies for Large systems, Grounding for mixed signal systems, Filter types and operation, Surge protection devices, Transient Protection.

UNIT IV STANDARD AND REGULATION 9

Need for Standards, Generic/General Standards for Residential and Industrial environment, Basic Standards, Product Standards, National and International EMI Standardizing Organizations; IEC, ANSI, FCC, AS/NZS, CISPR, BSI, CENELEC, ACEC. Electro Magnetic Emission and susceptibility standards and specifications, MIL461E Standards.

UNIT V EMI TEST METHODS AND INSTRUMENTATION 9

Fundamental considerations, EMI Shielding effectiveness tests, Open field test, TEM cell for immunity test, Shielded chamber , Shielded anechoic chamber, EMI test receivers, Spectrum analyzer, EMI test wave simulators, EMI coupling networks, Line impedance stabilization networks, Feed through capacitors, Antennas, Current probes, MIL -STD test methods, Civilian STD test methods.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of this course, the student should be able to:

- Identify Standards
- Compare EMI test methods
- Discuss EMI mitigation techniques

REFERENCES:

1. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3rd Ed, Artech house, Norwood, 1986.
2. Clayton Paul, “Introduction to Electromagnetic Compatibility”, Wiley Interscience, 2006.
3. Daryl Gerke and William Kimmel, “EDN"s Designer"s Guide to Electromagnetic Compatibility”, Elsevier Science & Technology Books, 2002
4. Dr Kenneth L Kaiser, “The Electromagnetic Compatibility Handbook”, CRC Press 2005.
5. Electromagnetic Compatibility by Norman Violette ,Published by Springer, 2013
6. Electromagnetic Interference and Compatibility: Electrical noise and EMI specifications Volume 1 of A Handbook Series on Electromagnetic Interference and Compatibility, Donald R. J. White Publisher-Don white consultants Original from the University of Michigan Digitized 6 Dec 2007
7. Henry W. Ott, “Electromagnetic Compatibility Engineering”, John Wiley & Sons Inc, Newyork, 2009
8. V Prasad Kodali, “Engineering Electromagnetic Compatibility”, IEEE Press, Newyork, 2001.
9. W Scott Bennett, “Control and Measurement of Unintentional Electromagnetic Radiation”, John Wiley & Sons Inc., (Wiley Interscience Series) 1997.

AP5003 VLSI DESIGN TECHNIQUES L T P C

3 0 0 3

OBJECTIVES:

- This course deals comprehensively with all aspects of transistor level design of all the digital building blocks common to all CMOS microprocessors, DPSs, network processors, digital backend of all wireless systems etc.
- The focus will be on the transistor level design and will address all important issues related to size, speed and power consumption. The units are classified according to the important building and will introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Nonbistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V INTERCONNECT AND CLOCKING STRATEGIES 6

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.
- Discuss design methodology of arithmetic building block
- Analyze tradeoffs of the various circuit choices for each of the building block.

REFERENCES:

1. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010.
2. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Prentice Hall of India 2nd Edition, Feb 2003,
3. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
4. N.Weste, K. Eshraghian, "Principles of CMOS VLSI Design". Addision Wesley, 2nd Edition, 1993

AP5071 NANOELECTRONICS L T P C
3 0 0 3

OBJECTIVES

- To understand how transistor as Nano device
- To understand various forms of Nano Devices
- To understand the Nano Sensors

UNIT I SEMICONDUCTOR NANO DEVICES 9

Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single-Electron Transistors; Nanorobotics and Nanomanipulation; Mechanical Molecular Nanodevices; Nanocomputers: Optical Fibers for Nanodevices; Photochemical Molecular Devices; DNA-Based Nanodevices; Gas-Based Nanodevices.

UNIT II ELECTRONIC AND PHOTONIC MOLECULAR MATERIALS 9

Preparation – Electroluminescent Organic materials - Laser Diodes - Quantum well lasers:- Quantum cascade lasers- Cascade surface-emitting photonic crystal laser- Quantum dot lasers - Quantum wire lasers:- White LEDs - LEDs based on nanowires - LEDs based on nanotubes - LEDs based on nanorods - High Efficiency Materials for OLEDs- High Efficiency Materials for OLEDs - Quantum well infrared photo detectors.

UNIT III THERMAL SENSORS 9

Thermal energy sensors -temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors.

UNIT IV GAS SENSOR MATERIALS 9

Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity; Discussion of sensors for various gases, Gas sensors based on semiconductor devices.

UNIT V BIOSENSORS 9

Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential.

TOTAL: 45 PERIODS

OUTCOMES:

- To be able to simulate and design the nano device
- To be able to simulate and design the nano sensors

REFERENCES:

1. K.E. Drexler, “Nano systems”, Wiley,1992.
2. M.C. Petty, “Introduction to Molecular Electronics”, 1995.
3. W. Ranier, “Nano Electronics and Information Technology”, Wiley, 2003.

CU5097 WIRELESS ADHOC AND SENSOR NETWORKS

L	T	P	C
3	0	0	3

OBJECTIVES:

- To understand the basics of Ad-hoc & Sensor Networks.
- To learn various fundamental and emerging protocols of all layers.
- To study about the issues pertaining to major obstacles in establishment and efficient management of Ad-hoc and sensor networks.
- To understand the nature and applications of Ad-hoc and sensor networks.
- To understand various security practices and protocols of Ad-hoc and Sensor Networks.

UNIT I MAC & TCP IN AD HOC NETWORKS 9

Fundamentals of WLANs – IEEE 802.11 Architecture - Self configuration and Auto configuration-Issues in Ad-Hoc Wireless Networks – MAC Protocols for Ad-Hoc Wireless Networks – Contention Based Protocols - TCP over Ad-Hoc networks-TCP protocol overview - TCP and MANETs – Solutions for TCP over Ad-Hoc Networks.

UNIT II ROUTING IN AD HOC NETWORKS 9

Routing in Ad-Hoc Networks- Introduction-Topology based versus Position based Approaches-Proactive, Reactive, Hybrid Routing Approach-Principles and issues – Location services - DREAM – Quorums based location service – Grid – Forwarding strategies – Greedy packet forwarding – Restricted directional flooding- Hierarchical Routing- Issues and Challenges in providing QoS.

UNIT III MAC, ROUTING & QOS IN WIRELESS SENSOR NETWORKS 9

Introduction – Architecture - Single node architecture – Sensor network design considerations – Energy Efficient Design principles for WSNs – Protocols for WSN – Physical Layer : Transceiver Design considerations – MAC Layer Protocols – IEEE 802.15.4 Zigbee – Link Layer and Error Control issues - Routing Protocols – Mobile Nodes and Mobile Robots - Data Centric & Contention Based Networking – Transport Protocols & QOS – Congestion Control issues – Application Layer support.

UNIT IV SENSOR MANAGEMENT 9

Sensor Management - Topology Control Protocols and Sensing Mode Selection Protocols - Time synchronization - Localization and positioning – Operating systems and Sensor Network programming – Sensor Network Simulators.

UNIT V SECURITY IN AD HOC AND SENSOR NETWORKS 9

Security in Ad-Hoc and Sensor networks – Key Distribution and Management – Software based Anti-tamper techniques – water marking techniques – Defense against routing attacks - Secure Adhoc routing protocols – Broadcast authentication WSN protocols – TESLA – Biba – Sensor Network Security Protocols – SPINS.

TOTAL : 45 PERIODS

OUTCOMES:

Upon Completion of the course, the students should be able to

- Identify different issues in wireless ad hoc and sensor networks.
- To analyze protocols developed for ad hoc and sensor networks.
- To identify and address the security threats in ad hoc and sensor networks.
- Establish a Sensor network environment for different type of applications.

REFERENCES:

1. Adrian Perrig, J. D. Tygar, "Secure Broadcast Communication: In Wired and Wireless Networks", Springer, 2006.
2. Carlos De Morais Cordeiro, Dharma Prakash Agrawal “Ad Hoc and Sensor Networks: Theory and Applications (2nd Edition), World Scientific Publishing, 2011
3. C.Siva Ram Murthy and B.S.Manoj, “Ad Hoc Wireless Networks – Architectures and Protocols”, Pearson Education, 2004.
4. C.K.Toh, “Ad Hoc Mobile Wireless Networks”, Pearson Education, 2002.
5. Erdal Çayırcı , Chunming Rong, “Security in Wireless Ad Hoc and Sensor Networks”, John Wiley and Sons, 2009.
6. Holger Karl, Andreas willig, Protocols and Architectures for Wireless Sensor Networks, John Wiley & Sons, Inc .2005.
7. Subir Kumar Sarkar, T G Basavaraju, C Puttamadappa, “Ad Hoc Mobile Wireless Networks”, Auerbach Publications, 2008.
8. Waltenegus Dargie, Christian Poellabauer, “Fundamentals of Wireless Sensor Networks Theory and Practice”, John Wiley and Sons, 2010.

AP5004 HIGH PERFORMANCE NETWORKS L T P C
3 0 0 3

OBJECTIVES:

- To develop a comprehensive understanding of multimedia networking.
- To study the types of VPN and tunneling protocols for security.
- To learn about network security in many layers and network management.

UNIT I INTRODUCTION 9

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET – DWDM – DSL – ISDN – BISDN,ATM.

UNIT II MULTIMEDIA NETWORKING APPLICATIONS 9

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP- differentiated services.

UNIT III ADVANCED NETWORKS CONCEPTS 9

VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS- operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks-P2P connections.

UNIT IV TRAFFIC MODELLING 9

Little's theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, Network performance evaluation.

UNIT V NETWORK SECURITY AND MANAGEMENT 9

Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1

TOTAL: 45PERIODS

OUTCOMES:

Upon completion of this course, the students should be able to:

- Discuss advanced networks concepts
- Outline traffic modeling
- Evaluate network security

REFERENCES:

1. Aunurag Kumar, D. M Anjunath, Joy Kuri, "Communication Networking", Morgan Kaufmann Publishers, 1st edition 2004.
2. Fred Halsall and Lingana Gouda Kulkarni, "Computer Networking and the Internet", fifth edition, Pearson education 2006
3. Hersent Gurle & Petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson education 2003
4. J.F. Kurose & K.W. Ross,"Computer Networking- A top down approach featuring the internet", Pearson, 2nd edition, 2003
5. Larry l.Peterson & Bruce S.David, "Computer Networks: A System Approach"- 1996
6. LEOM-GarCIA, WIDJAJA, "Communication networks", TMH seventh reprint 2002.
7. Nader F.Mir ,Computer and Communication Networks, first edition 2010
8. Walrand .J. Varatya, High performance communication network, Morgan Kauffman – Harcourt Asia Pvt. Ltd. 2nd Edition, 2000

DS5191	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C
		3	0	0	3

OBJECTIVES:

The objective of this course is to provide in-depth knowledge on

- Digital Signal Processor basics
- Third generation DSP Architecture and programming skills
- Advanced DSP architectures and some applications.

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs 9

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

UNIT II TMS320C5X PROCESSOR 9

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

UNIT III TMS320C6X PROCESSOR 9

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.

UNIT IV ADSP PROCESSORS 9

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

UNIT V ADVANCED PROCESSORS 9

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL : 45 PERIODS

OUTCOMES:

Students should be able to:

- Become Digital Signal Processor specialized engineer
- DSP based System Developer

REFERENCES:

1. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, cengage Learning India Private Limited, Delhi 2012
2. B.Venkataramani and M.Bhaskar, “Digital Signal Processors – Architecture, Programming and Applications” – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
3. RulphChassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, A JOHN WILEY & SONS, INC., PUBLICATION, 2005
4. User guides Texas Instrumentation, Analog Devices, Motorola.

AP5073 **RF SYSTEM DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- The CMOS RF Front End (RFE) is a very crucial building block and in all of wireless and many high frequency wire-line systems. The RFE has few important building blocks within ii including the Low Noise Amplifiers, Phase Locked Loop Synthesizers, Mixers, Power Amplifiers, and impedance matching circuits.
- The present course will introduce the principles of operation and design principles associated with these important blocks.
- The course will also provide and highlight the appropriate digital communication related design objectives and constraints associated with the RFEs

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES **9**

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter.

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS **9**

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS **9**

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearisation Techniques, Efficiency boosting techniques, ACPR metric, Design considerations.

UNIT IV MIXERS AND OSCILLATORS **9**

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS **9**

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TOTAL : 45 PERIODS

OUTCOMES:

- The student after completing this course must be able to translate the top level wireless communications system specifications into block level specifications of the RFE.
- The student should be also able to carry out transistor level design of the entire RFE.

REFERENCES:

1. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4. Recorded lectures and notes available at . http://www.ee.iitm.ac.in/~ani/ee6240/
5. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.

AP5074 SPEECH AND AUDIO SIGNAL PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To study basic concepts of processing speech and audio signals
- To study and analyse various M-band filter-banks for audio coding
- To understand audio coding based on transform coders.
- To study time and frequency domain speech processing methods

UNIT I MECHANICS OF SPEECH AND AUDIO 9

Introduction - Review of Signal Processing Theory-Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Absolute Threshold of Hearing - Critical Bands- Simultaneous Masking, Masking-Asymmetry, and the Spread of Masking- Non-simultaneous Masking - Perceptual Entropy - Basic measuring philosophy -Subjective versus objective perceptual testing - The perceptual audio quality measure (PAQM) - Cognitive effects in judging audio quality.

UNIT II TIME-FREQUENCY ANALYSIS: FILTER BANKS AND TRANSFORMS 9

Introduction - Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations - Quadrature Mirror and Conjugate Quadrature Filters - Tree-Structured QMF and CQF M-band Banks - Cosine Modulated “Pseudo QMF” M-band Banks -Cosine Modulated Perfect Reconstruction (PR) M-band Banks and the Modified Discrete Cosine
Transform (MDCT) - Discrete Fourier and Discrete Cosine Transform - Pre-echo Distortion- Pre-echo Control Strategies

UNIT III AUDIO CODING AND TRANSFORM CODERS 9

Lossless Audio Coding – Lossy Audio Coding - ISO-MPEG-1A, 2A, 2A-Advaned, 4A Audio Coding - Optimum Coding in the Frequency Domain - Perceptual Transform Coder –Brandenburg - Johnston Hybrid Coder - CNET Coders - Adaptive Spectral Entropy Coding –Differential Perceptual Audio Coder - DFT Noise Substitution -DCT with Vector Quantization -MDCT with Vector Quantization

UNIT IV TIME AND FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING 9

Time domain parameters of Speech signal – Methods for extracting the parameters :Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy Short Time Fourier analysis – Formant extraction – Pitch Extraction using time and frequency domain methods Homomorphic Speech Analysis: Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders

UNIT V PREDICTIVE ANALYSIS OF SPEECH 9

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin’s Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP

TOTAL : 45 PERIODS

OUTCOMES:

Upon completion of this course, the students should be able to:

- Evaluate audio coding and transform coders
- Discuss time and frequency domain methods for speech processing
- Explain predictive analysis of speech

REFERENCES:

1. B.Gold and N.Morgan, “Speech and Audio Signal Processing”, Wiley and Sons, 2000.
2. L.R.Rabiner and R.W.Schaffer, "Digital Processing of Speech Signals", Prentice Hall, 1978.
3. Mark Kahrs, Karlheinz Brandenburg, Kluwer Applications of Digital Signal Processing to Audio And Acoustics, Academic Publishers,
4. Udo Zölzer, "Digital Audio Signal Processing", Second Edition A John Wiley& sons Ltd

AP5092 SOLID STATE DEVICE MODELLING AND SIMULATION L T P C
3 0 0 3

OBJECTIVES:

- To understand the concept of device modeling
- To learn multistep method
- To study device simulations

UNIT I MOSFET DEVICE PHYSICS MOSFET 9

capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II DEVICE MODELLING 9

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

UNIT III MULTISTEP METHODS 9

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT IV MATHEMATICAL TECHNIQUES DEVICE SIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V SIMULATION OF DEVICES 9

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

TOTAL :45PERIODS

OUTCOMES:

Upon completion of this course, the students should be able to:

- Explain the importance of MOS Capacitor and Small signal modeling
- Apply and determine the drift diffusion equation and stiff system equation.
- Analyze circuits using parasitic BJT parameters and newton Raphson method.
- Model the MOS transistor using schrodinger equation and Multistep methods.

REFERENCES:

1. Arora, N., “MOSFET Modeling for VLSI Simulation”, Cadence Design Systems, 2007
2. Chua, L.O. and Lin, P.M., “Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques”, Prentice-Hall., 1975
3. Fjeldly, T., Yetterdal, T. and Shur, M., “Introduction to Device Modeling and Circuit Simulation”, Wiley-Interscience., 1997
4. Grasser, T., “Advanced Device Modeling and Simulation”, World Scientific Publishing Company., 2003
5. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer- Verlag.,1984
6. Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd.

CP5292 INTERNET OF THINGS

L	T	P	C
3	0	0	3

OBJECTIVES:

- To understand the fundamentals of Internet of Things
- To learn about the basics of IOT protocols
- To build a small low cost embedded system using Raspberry Pi.
- To apply the concept of Internet of Things in the real world scenario

UNIT I INTRODUCTION TO IoT **9**

Internet of Things - Physical Design- Logical Design- IoT Enabling Technologies - IoT Levels & Deployment Templates - Domain Specific IoTs - IoT and M2M - IoT System Management with NETCONF-YANG- IoT Platforms Design Methodology

UNIT II IoT ARCHITECTURE **9**

M2M high-level ETSI architecture - IETF architecture for IoT - OGC architecture - IoT reference model - Domain model - information model - functional model - communication model - IoT reference architecture

UNIT III IoT PROTOCOLS **9**

Protocol Standardization for IoT – Efforts – M2M and WSN Protocols – SCADA and RFID Protocols – Unified Data Standards – Protocols – IEEE 802.15.4 – BACNet Protocol – Modbus– Zigbee Architecture – Network layer – 6LowPAN - CoAP - Security

UNIT IV BUILDING IoT WITH RASPBERRY PI & ARDUINO **9**

Building IOT with RASPERRY PI- IoT Systems - Logical Design using Python – IoT Physical Devices & Endpoints - IoT Device -Building blocks -Raspberry Pi -Board - Linux on Raspberry Pi - Raspberry Pi Interfaces -Programming Raspberry Pi with Python - Other IoT Platforms - Arduino.

UNIT V CASE STUDIES AND REAL-WORLD APPLICATIONS **9**

Real world design constraints - Applications - Asset management, Industrial automation, smart grid, Commercial building automation, Smart cities - participatory sensing - Data Analytics for IoT – Software & Management Tools for IoT Cloud Storage Models & Communication APIs - Cloud for IoT - Amazon Web Services for IoT.

TOTAL :45 PERIODS

OUTCOMES:

Upon completion of this course, the students should be able to:

- Analyze various protocols for IoT
- Develop web services to access/control IoT devices.
- Design a portable IoT using Rasperry Pi
- Deploy an IoT application and connect to the cloud.
- Analyze applications of IoT in real time scenario

REFERENCES:

1. Arshdeep Bahga, Vijay Madisetti, “Internet of Things – A hands-on approach”, Universities Press, 2015
2. Dieter Uckelmann, Mark Harrison, Michahelles, Florian (Eds), “Architecting the Internet of Things”, Springer, 2011.
3. Honbo Zhou, “The Internet of Things in the Cloud: A Middleware Perspective”, CRC Press, 2012.
4. Jan Ho¨ ller, Vlasios Tsiatsis , Catherine Mulligan, Stamatis , Karnouskos, Stefan Avesand. David Boyle, "From Machine-to-Machine to the Internet of Things - Introduction to a New Age of Intelligence", Elsevier, 2014.
5. Olivier Hersent, David Boswarthick, Omar Elloumi , “The Internet of Things – Key applications and Protocols”, Wiley, 2012

AP5005	SYSTEM ON CHIP DESIGN	L	T	P	C
		3	0	0	3

OBJECTIVES:

- understanding of the concepts, issues, and process of designing highly integrated SoCs following systematic hardware/software co-design & co-verification principles

UNIT I INTRODUCTION 9

Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middle ware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design

UNIT II SYSTEM LEVEL MODELLING 9

SystemC: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples

UNIT III HARDWARE SOFTWARE CO-DESIGN 9

Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems.

UNIT IV SYNTHESIS 9

System synthesis: Transaction Level Modelling (TLM) based design, automaticTLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimisation, resource sharing and pipelining and scheduling

UNIT V SOC VERIFICATION AND TESTING 9

SoC and IP integration, Verification : Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modeling, test power dissipation, test access mechanism

TOTAL : 45 PERIODS

OUTCOMES:

- Analyse algorithms and architecture of hardware software inorder to optimise the system based on requirements and implementation constraints
- Model and specify systems at high level of abstraction
- appreciate the co-design approach and virtual platform models
- Understand hardware, software and interface synthesis

REFERENCES

1. D. Black, J. Donovan, SystemC: From the Ground Up, Springer, 2004.
2. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling, Synthesis, Verification, Springer, 2009
3. Erik Larson, Introduction to advanced system-on-chip test design and optimisation, Springer 2005
4. Grotker, T., Liao, S., Martin, G. & Swan, S. System design with System C, Springer, 2002.
5. Ghenassia, F. Transaction-level modeling with SystemC: TLM concepts and applications for embedded systems, Springer, 2010.
6. Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, “Low power NoC for high performance SoCdesing”,CRC press, 2008.
7. M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2005
8. M. Abramovici, M. Breuer, and A. Friedman, Digital System Testing and Testable Design, IEEE Press, 1994
9. P. Marwedel, Embedded System Design, Springer, 2003. G. De Micheli, Synthesis and Optimization of Digital Circuits
10. Prakash Rashinkar, Peter Paterson and Leena Singh, System-on-a chip verification: Methodology and techniques, kluwer Academic Publishers 2002
11. T. Noergaard, Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers, Newnes.
12. Vijay K. MadisettiChonlamethArpikanondt, “A Platform-Centric Approach to System-on-Chip (SOC) Design”, Springer, 2005.
13. Youn-Long Steve Lin, Essential Issues in SOC Design Designing Complex Systems-on-Chip, Springer, 2006

AP5093	ROBOTICS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To understand robot locomotion and mobile robot kinematics
- To understand perception in robotics
- To understand mobile robot localization
- To understand mobile robot mapping
- To understand simultaneous localization and mapping (SLAM)
- To understand robot planning and navigation

UNIT I LOCOMOTION AND KINEMATICS 9

Introduction to Robotics – key issues in robot locomotion – legged robots – wheeled mobile robots – aerial mobile robots – introduction to kinematics – kinematics models and constraints – robot maneuverability

UNIT II ROBOT PERCEPTION 9

Sensors for mobile robots – vision for robotics – cameras – image formation – structure from stereo – structure from motion – optical flow – color tracking – place recognition – range data

UNIT III MOBILE ROBOT LOCALIZATION 9

Introduction to localization – challenges in localization – localization and navigation – belief representation – map representation – probabilistic map-based localization – Markov localization – EKF localization – UKF localization – Grid localization – Monte Carlo localization – localization in dynamic environments

UNIT IV MOBILE ROBOT MAPPING 9

Autonomous map building – occupancy grip mapping – MAP occupancy mapping – SLAM –extended Kalman Filter SLAM – graph-based SLAM – particle filter SLAM – sparse extended information filter – fastSLAM algorithm.

UNIT V PLANNING AND NAVIGATION 9

Introduction to planning and navigation – planning and reacting – path planning – obstacle avoidance techniques – navigation architectures – basic exploration algorithms

TOTAL 45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- Explain robot locomotion
- Apply kinematics models and constraints
- Implement vision algorithms for robotics
- Implement robot localization techniques
- Implement robot mapping techniques
- Implement SLAM algorithms
- Explain planning and navigation in robotics

REFERENCES:

1. Gregory DudekandMichael Jenkin, “Computational Principles of Mobile Robotics”, Second Edition, Cambridge University Press, 2010.
2. Howie Choset et al., “Principles of Robot Motion: Theory, Algorithms, and Implementations”, A Bradford Book, 2005.
3. Maja J. Mataric, “The Robotics Primer”, MIT Press, 2007.
4. Roland Seigwart, Illah Reza Nourbakhsh, and Davide Scaramuzza, “Introduction to autonomous mobile robots”, Second Edition, MIT Press, 2011.
5. Sebastian Thrun, Wolfram Burgard, and Dieter Fox, “Probabilistic Robotics”, MIT Press, 2005.

AP5006 PHYSICAL DESIGN OF VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To introduce the physical design concepts such as routing, placement, partitioning and packaging
- To study the performance of circuits layout designs, compaction techniques.

UNIT I INTRODUCTION TO VLSI TECHNOLOGY 9

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies Packaging-Computational Complexity - Algorithmic Paradigms.

UNIT II PLACEMENT USING TOP-DOWN APPROACH 9

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut partition with capacity and i/o constrants. Floor planning: Rectangular dual floor planning hierarchical approach- simulated annealing- Floor plan sizing Placement: Cost function- force directed method-placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement.

UNIT III ROUTING USING TOP DOWN APPROACH 9

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches - hierarchial approaches - multi commodity flow based techniques - Randomised Routing- One Step approach - Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization

UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION 9

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing Multiple chip modules(MCM)-programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

TOTAL: 45 PERIODS

OUTCOMES:

Upon Completion of the course, the students will be able to

- Explain different types of routing
- Discuss performance issues in circuit layout
- Outline 1D compaction- 2D compaction.

REFERENCES:

1. Preas M. Lorenzatti, “Physical Design and Automation of VLSI systems”, The Benjamin Cummins Publishers, 1998.
2. Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, McGraw Hill Int. Edition 1995

AP5094 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossles models

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL : 45 PERIODS

OUTCOMES:

- Ability to identify sources affecting the speed of digital circuits.
- Able to improve the signal transmission characteristics.

REFERENCES:

1. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR, 2003
2. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.
3. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
4. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.

TOOLS REQUIRED

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

VL5091	MEMS AND NEMS	L T P C
		3 0 0 3

OBJECTIVES:

- To introduce the concepts of microelectromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To familiarize concepts of quantum mechanics and nano systems.

UNIT I OVERVIEW **9**

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT II MEMS FABRICATION TECHNOLOGIES **9**

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

UNIT III MICRO SENSORS **9**

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV MICRO ACTUATORS **9**

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS **9**

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of this course, the student should be able to:

- Discuss micro sensors
- Explain micro actuators
- Outline nanosystems and Quantum mechanics

REFERENCES:

1. Chang Liu, “Foundations of MEMS”, Pearson education India limited, 2006.
2. Marc Madou, “Fundamentals of Microfabrication”, CRC press 1997
3. Stephen D. Senturia,” Micro system Design”, Kluwer Academic Publishers,2001
4. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures” CRC Press, 2002.
5. Tai Ran Hsu ,"MEMS and Microsystems Design and Manufacture” ,Tata McGraw Hill, 2002

AP5007	SECURE COMPUTING SYSTEMS	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn computer hardware, system software and data concepts from a security perspective

UNIT I UNIT I COMPUTER SECURITY AND MANAGEMENT 9

Overview of Computer Security, Threats, Malware, Vulnerabilities, Authentication, Access Control, Security Management Models, Security Management Practices, Protection Mechanisms, Legal aspects of security, Ethical Hacking.

UNIT II HARDWARE SECURITY 9

Need for Hardware Security, Computer Memory and storage, Bus and Interconnection, I/O and Network Interface, CPU; Side channel Analysis: Power Analysis Attack, Timing Attack, Fault attack. Countermeasures of Side Channel Attack, Secure Hardware Intellectual Properties, Physically Unclonable Functions(PUFs), Secure PUF.

UNIT III ASSEMBLY AND OPERATING SYSTEMS SECURITY 9

Opcode, Operands, Addressing Modes, Stack and Buffer Overflow, FIFO and M/M/1 Problem, Kernel, Drivers and OS Security; Secure Design Principles, Trusted Operating Systems, Trusted System Functions

UNIT IV ADVANCED COMPUTER ARCHITECTURE 9

Security aspects : Multiprocessors, parallel processing, Ubiquitous computing, Grid, Distributed and cloud computing, Internet computing, Virtualization

UNIT V NETWORK AND WEBSECURITY 9

TCP/IP Protocol, Network switches, Routers, Gateways, Wireless Networks and Network Address Translation (NAT); Network Security Issues in TCP/IP, Threat Models, Denial of Service Attacks, Firewalls, Intrusion Detection, Browser Attacks, Web Attacks Targeting Users, Email Attacks, Secure Shell (SSH), HTTPS

TOTAL : 45 PERIODS

OUTCOMES:

- Aware of Security aspects
- Able to appreciate security in hardware, OS and it future need
- Learn security issues in various types of computing networks

REFERENCES:

1. Charles B. Pfleeger, Shari Lawrence Pfleeger, “Security in Computing”, Fourth Edition, Pearson Education, 2007
2. Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, “Hardware Security - Design Threats and Safeguards”, CRC Press, 2015
3. Michael Whitman, Herbert J. Mattord, “Management of Information Security”, Third Edition, Course Technology, 2010
4. Shuangbao Wang, Robert S.Ledley, Computer Architecture and Security, Wiley, 2013
5. William Stallings, “Network Security Essentials, Applications and Standards”, Dorling Kindersley I P Ltd, Delhi, 2008.

AP5008	PATTERN RECOGNITION	L	T	P	C
		3	0	0	3

OBJECTIVES:

- To learn about supervised and unsupervised pattern classifiers.
- To familiarize about different feature extraction techniques.
- To explore the role of Hidden Marko model and SVM in pattern recognition.
- To understand the application of Fuzzy logic and genetic algorithms for pattern classifier

UNIT I PATTERN CLASSIFIER **9**

Overview of Pattern recognition – Discriminant functions – Supervised learning – Parametric estimation – Maximum Likelihood Estimation – Bayesian parameter Estimation – Problems with Bayes approach– Pattern classification by distance functions – Minimum distance pattern classifier.

UNIT II CLUSTERING **9**

Clustering for unsupervised learning and classification–Clustering concept – C Means algorithm – Hierarchical clustering – Graph theoretic approach to pattern Clustering – Validity of Clusters.

UNIT III FEATURE EXTRACTION AND STRUCTURAL PATTERN RECOGNITION **9**

Principle component analysis, Independent component analysis, Linear discriminant analysis, Feature selection through functional approximation – Elements of formal grammars, Syntactic description – Stochastic grammars – Structural Representation.

UNIT IV HIDDEN MARKOV MODELS AND SUPPORT VECTOR MACHINE **9**

State Machines – Hidden Markov Models – Training – Classification – Support vector Machine – Feature Selection.

UNIT V RECENT ADVANCES **9**

Fuzzy logic – Fuzzy Pattern Classifiers – Pattern Classification using Genetic Algorithms – Case Study Using Fuzzy Pattern Classifiers and Perception.

TOTAL : 45 PERIODS

OUTCOMES:

Upon completion of the course the student will be able to

- Differentiate between supervised and unsupervised classifiers
- Classify the data and identify the patterns.
- Extract feature set and select the features from given data set.
- Apply fuzzy logic and genetic algorithms for classification problems

REFERENCES:

1. Andrew Webb, "Stastical Pattern Recognition", Arnold publishers, London,1999
2. C.M.Bishop, "Pattern Recognition and Machine Learning", Springer, 2006.
3. M. Narasimha Murthy and V. Susheela Devi, "Pattern Recognition", Springer 2011.
4. Menahem Friedman , Abraham Kandel, "Introduction to Pattern Recognition Statistical, Structural, Neural and Fuzzy Logic Approaches", World Scientific publishing Co. Ltd, 2000.
5. Robert J.Schalkoff, "Pattern Recognition Statistical, Structural and Neural Approaches", John Wiley & Sons Inc., New York, 1992.
6. R.O.Duda, P.E.Hart and D.G.Stork, "Pattern Classification", John Wiley, 2001
7. S.Theodoridis and K.Koutroumbas, "Pattern Recognition", 4th Ed., Academic Press. 2009.