

**ELECTRONICS AND
COMMUNICATION ENGINEERING**

Requisition Letter

From,

Head of the Department,
Department of Electronics and Communication Engineering,
J.K.K.Munirajah College of Technology,
T.N.Palayam.

To,

The Principal,
J.K.K.Munirajah College of Technology,
T.N.Palayam.

Permitted
Sreed 28/8/21

Respected Sir,

Sub: Seeking permission for conducting a Certificate Program-Reg

We have planned to conduct a certificate program for II-, III- and IV-year ECE students on "RTL Design and Verification" from 23.08.2021 to 28.08.2021 by program coordinator Mrs.R.Kokila AP/ECE. So, I request you to kindly provide permission to conduct the certificate program.

Thanking You,

Yours Truly,

Place: T.N.Palayam

Date: 12.08.2021

Sreed

Sreed 12/8/21

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JKKMCT/CIRCULAR/47/AUG-2021

DATE: 13/08/2021

CIRCULAR

The Department of Electronics and Communication Engineering is planning to organize a Certificate Program on “RTL Design and Verification” (36 Hours) for the benefit of the students from 23.08.2021 (Monday) to 28.08.2021 (Saturday). Students those who are willing to attend the program can enroll their names to their class in-charges respectively on or before 16.08.2021.



PRINCIPAL 13/8/21

Copy To,

All the HODs and Staff Members,

The Student's circulation,

Notice boards and File copy


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Department of Electronics and Communication Engineering

PROGRAM SYLLABUS

Name of the Certificate Program : RTL Design and Verification

Program Code : 21ECERTLDVCP01

Name of the Program Coordinator : Mrs.R.Kokila

Academic Year: 2021-2022

Program Contents

Total Hours: 36

Chapter 1 : Digital logic Fundamentals and Advanced Digital Design

- Importance and advantages of digital electronics
- Digital Number System, Binary logic gates & Boolean algebra
- Combinational and Sequential circuit designs
- Evolution of the Sequential Elements-Latches and Flip Flops
- Design of Synchronous Sequential Machines-Synchronous Detectors, Counters and Registers
- Design of Hybrid Counters
- Design of complex Sequence detectors
- Design of Control FSMs based on the specifications
- Design of Frequency synthesizers

Chapter 2 : CMOS Basics and ASIC/FPGA/SOC Design Flow

- Acquire the knowledge about various CMOS fabrication process
- NMOS and PMOS operation
- CMOS characteristics
- CMOS inverter rise, fall and propagation delays
- CMOS second order effects
- Analyse and implement various functions using CMOS circuits
- CMOS Flip flop and its timing parameters
- Overview of FPGA/ASIC/SOC design flow
- FPGA Vs ASIC comparison

Chapter 3 : RTL Design using System Verilog HDL

- Understanding RTL Design.
- Understanding basics of CDC and DFT
- System Verilog data types



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- System Verilog procedural blocks and statements
- Usage of System Verilog Interface in RTL design
- Parameterized Interfaces and Modports
- Usage of Generate and Genvar in RTL design for multi-master and multi-slave configuration
- Design of synchronous machines using System Verilog

Chapter 4 : RTL Synthesis and Logic Equivalence Checks (LEC)

- Introduction to Synthesis
- Data Setup for DC
- Accessing Design and Library Objects
- Constraints: Reg-to-Reg and I/O Timing
- Constraints: Input Transition and Output Loading
- Constraints: Multiple Clocks and Exceptions
- Constraints: Complex Design Considerations
- Post-Synthesis Output Data
- Basic concepts of Formal verification and LEC
- Input generation for LEC

Chapter 5 : RTL Verification using VERILOG HDL

- Understanding Verification types
- Verification flow
- Test bench architecture
- Developing Test bench components
- Simulation and Synthesis mis-matches,
- Test bench models
- Understanding X-propagation,
- Timing Verification-Gate level simulation
- Hands on project

Prepared by:

Name: Mrs.R.Kokila

Designation: AP/ ECE


PROGRAM COORDINATOR


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Department of Electronics and Communication Engineering

Academic Year 2021-2022

Certificate Program on "RTL Design and Verification"

Schedule Plan

Dates	09:30 AM to 11:30 AM (2 Hrs)	BREAK	11.45 AM to 1.15 PM (1.30 Hrs)	LUNCH	2:00 PM to 4.30 PM (2.30 Hrs)
23.08.2021	Introduction and Digital logic Fundamentals		Design of Synchronous Sequential Machines- Synchronous Detectors, Counters and Registers		Design of complex Sequence detectors and Frequency synthesizers
24.08.2021	CMOS Basics		Analyse and implement various functions using CMOS circuits		ASIC/FPGA/SOC Design Flow
25.08.2021	RTL Design using System Verilog HDL		Usage of System Verilog Interface in RTL design		Usage of Generate and Genvar in RTL design for multi-master and multi-slave configuration
26.08.2021	Design of synchronous machines using System Verilog		Design of memory block using System Verilog		RTL Synthesis
27.08.2021	Constraints: Reg-to-Reg and I/O Timing, , Multiple Clocks and Exceptions, Complex Design Considerations		Logic Equivalence Checks		RTL Verification using VERILOG HDL
28.08.2021	Test bench architecture, Developing Test bench components, Test bench models.		Hands on project		Hands on project Questions and feedback

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Department of Electronics and Communication Engineering

Academic Year 2021-2022

Resource Person Profile

Title of the Program	RTL Design and Verification
Duration and Timing of the Program	36 Hours & 9.30 AM to 4.30 PM
Name of the Resource Person	Mrs.R.KOKILA
Photo Image of the Resource Person	
E-mail	kokilaece89@gmail.com
Mobile No	9976507503
Designation	Assistant Professor / ECE
Official Address	Department of ECE, J.K.K.Munirajah College of Technology, T.N.Palayam, Gobi(tk), Erode(Dt) - 638506
Educational Qualification	B.E (Electronics and Communication Engineering), M.E (Applied Electronics)
Experience	Eight years of Teaching experience as an assistant professor in our college.
Field of Interest	Image processing, VLSI Design, Digital Electronics, Antennas and Microwave Engineering
Others	She presented papers in various conferences



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Department of Electronics and Communication Engineering

Academic Year 2021-2022

Certificate Program on "RTL Design and Verification"

Students Willing List

S.NO	REGISTER NUMBER	STUDENT NAME	WILLING STUDENTS SIGNATURE
FINAL YEAR			
1	731218106001	BABY SHALINI G	G. Baby
2	731218106002	DEEPAK M	M. Dhris
3	731218106003	DHARANI M	M. Dhris
4	731218106005	JAI SRI ADHITHYA T	Not Willing
5	731218106006	JEEVITHA P	P. Jeevitha
6	731218106009	KEERTHANA T	T. Keerthana
7	731218106012	PERIYASAMY T	Not Willing
8	731218106013	PRIYA R	R. Priya
9	731218106014	PRIYA V	V. Priya
10	731218106015	PRIYADHARSINI A	A. Melli
11	731218106016	RAMACHANDHIRAN G	G. Ramachandhiran
12	731218106017	SAKTHISUNDARAM D	D. Sayu
13	731218106018	SANTHIYA A	A. Santhiya
14	731218106301	MANIVEL M	M. Manivel
THIRD YEAR			
15	731219106001	BHARATHI M	M. Bharathi
16	731219106004	JAGADESHKUMAR G	G. Jagadeeshkumar
17	731219106006	KEMPARAJ K	Kemparaj
18	731219106008	MATHAN KUMAR M	M. Mathan
19	731219106009	MOHAN K	K. Mohan
20	731219106010	MUTHUPANDI M	M. Muthu
21	731219106011	NANDHINI P	P. Nandhini
22	731219106012	NARMATHA M	M. Narmatha
23	731219106014	RAMESH PRABHU R	R. Ramesh
24	731219106015	ROHINI M	M. Rohini
25	731219106016	SABARI GAYATHRI A	A. Sabari Gayathri
26	731219106018	SATHYAPRIYA K	K. Sathyapriya
27	731219106019	SURENDHAR P	P. Surendhar
28	731219106020	SURUTHIKA K	Not Willing
29	731219106021	UDHA YAKUMAR M	M. Udhayakumar
30	731219106301	KURALARASAN D	Not Willing



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SECOND YEAR			
31	731220106002	KALYAN K	K. K. K.
32	731220106004	KUDIYARASU P	P. K. K.
33	731220106005	MUTHUKUMAR M	M. M. M.
34	731220106007	SUGUNA DEVI M	S. D. M.
35	731220106008	VIKRAM V	NOT willing
36	731220206301	JANARTHANAN K	K. J. K.


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Department of Electronics and Communication Engineering

Academic Year 2021-2022

Certificate Program on "RTL Design and Verification"

Enrolled Students Name List

FINAL YEAR		
S.NO	REGISTER NUMBER	STUDENT NAME
1	731218106001	BABY SHALINI G
2	731218106002	DEEPAK M
3	731218106003	DHARANI M
4	731218106006	JEEVITHA P
5	731218106009	KEERTHANA T
6	731218106013	PRIYA R
7	731218106014	PRIYA V
8	731218106015	PRIYADHARSINI A
9	731218106016	RAMACHANDHIRAN G
10	731218106017	SAKTHISUNDARAM D
11	731218106018	SANTHIYA A
12	731218106301	MANIVEL M
THIRD YEAR		
13	731219106001	BHARATHI M
14	731219106004	JAGADESHKUMAR G
15	731219106006	KEMPARAJ K
16	731219106008	MATHAN KUMAR M
17	731219106009	MOHAN K
18	731219106010	MUTHUPANDI M
19	731219106011	NANDHINI P
20	731219106012	NARMATHA M
21	731219106014	RAMESH PRABHU R
22	731219106015	ROHINI M
23	731219106016	SABARI GAYATHRI A
24	731219106018	SATHYAPRIYA K
25	731219106019	SURENDHAR P
26	731219106021	UDHAYAKUMAR M
SECOND YEAR		
27	731220106002	KALYAN K
28	731220106004	KUDIYARASU P
29	731220106005	MUTHUKUMAR M
30	731220106007	SUGUNA DEVI M
31	731220206301	JANARTHANAN K


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Department of Electronics and Communication Engineering

Academic Year 2021-2022

Certificate Program on "RTL Design and Verification"

Attendance Details

S.NO	NAME OF THE STUDENT	ATTENDANCE OF THE PARTICIPANTS											
		23.08.2021		24.08.2021		25.08.2021		26.08.2021		27.08.2021		28.08.2021	
		FN	AN	FN	AN	FN	AN	FN	AN	FN	AN	FN	AN
FINAL YEAR													
1	BABY SHALINI G	/	/	/	/	/	/	/	/	/	/	/	/
2	DEEPAK M	/	/	/	/	/	/	/	/	/	/	/	/
3	DHARANI M	/	/	/	/	/	/	/	/	/	/	/	/
4	JEEVITHA P	/	/	/	/	/	/	/	/	/	/	/	/
5	KEERTHANA T	/	/	/	/	/	/	/	/	/	/	/	/
6	PRIYA R	/	/	/	/	/	/	/	/	/	/	/	/
7	PRIYA V	/	/	/	/	/	/	/	/	/	/	/	/
8	PRIYADHARSINI A	/	/	/	/	/	/	/	/	/	/	/	/
9	RAMACHANDHIRAN G	/	/	/	a	/	/	/	/	/	/	/	/
10	SAKTHISUNDARAM D	/	/	/	/	/	/	a	/	/	/	/	/
11	SANTHIYA A	/	/	/	/	/	/	/	/	/	/	/	/
12	MANIVEL M	/	/	/	/	/	a	/	/	/	/	/	/
THIRD YEAR													
13	BHARATHI M	/	/	/	/	/	/	/	/	/	/	/	/
14	JAGADESHKUMAR G	/	/	/	/	/	/	/	/	/	/	/	/
15	KEMPARAJ K	a	a	a	a	/	/	/	/	/	a	/	/
16	MATHAN KUMAR M	/	/	/	/	/	/	/	/	/	/	/	/
17	MOHAN K	/	/	/	/	/	/	/	/	/	/	/	/
18	MUTHUPANDI M	/	/	/	/	/	/	/	/	/	/	/	/
19	NANDHINI P	/	/	/	/	/	a	/	/	/	/	/	/
20	NARMATHA M	/	/	/	/	/	/	/	/	/	/	/	/
21	RAMESH PRABHU R	/	/	/	/	a	/	/	a	/	/	/	/
22	ROHINI M	/	/	a	a	a	a	/	a	a	/	/	/
23	SABARI GAYATHRI A	/	/	/	/	/	/	/	/	/	/	/	/
24	SATHYAPRIYA K	/	/	/	/	/	/	/	/	/	/	/	/
25	SURENDHAR P	/	a	/	/	/	/	/	/	/	/	/	/
26	UDHAYAKUMAR M	/	/	/	/	/	/	/	/	/	/	/	/
SECOND YEAR													
27	KALYAN K	/	/	/	/	/	/	/	/	/	/	/	/
28	KUDIYARASU P	/	/	/	/	/	/	/	/	/	a	/	/
29	MUTHUKUMAR M	/	/	/	/	/	/	/	/	/	/	/	/
30	SUGUNA DEVI M	/	a	/	a	/	/	a	a	a	a	a	/
31	JANARTHANAN K	/	/	/	/	/	/	/	/	/	/	/	/
Total No. of Present		30	28	29	27	29	28	29	28	29	28	30	31
Total No. of Absent		1	3	2	4	2	3	2	3	2	3	1	-
Signature of Program Coordinator													
Signature of HOD													

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Department of Electronics and Communication Engineering

Academic Year 2021-2022

Certificate Program on "RTL Design and Verification"

Assessment Details

1. RTL is a design abstraction of what kind of circuit?

- a) Asynchronous digital circuit
- b) Synchronous digital circuit
- c) Asynchronous sequential circuit
- d) Analog circuit

2. Which flip-flop is usually used in the implementation of the registers?

- a) D flip-flop
- b) S-R flip-flop
- c) T flip-flop
- d) J-K flip-flop

3. Hold time is the time needed for the data to _____ after the edge of the clock is triggered.

- a) Decrease
- b) Increase
- c) Remain constant
- d) Negate

4. The truth table which accurately explains the operation of CMOS not gate is:

a)

Input	pMOS	nMOS	Output
0	OFF	ON	1
1	OFF	ON	0

b)

Input	pMOS	nMOS	Output
0	ON	OFF	1
1	ON	OFF	0

c)

Input	pMOS	nMOS	Output
0	ON	ON	1
1	OFF	OFF	0

d)

Input	pMOS	nMOS	Output
0	ON	OFF	1
1	OFF	ON	0

5. RTL mainly focuses on describing the flow of signals between _____

- a) Logic gates
- b) Registers
- c) Clock
- d) Inverter



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6. What does RTL in digital circuit design stand for?

- a) Register transfer language
- b) Register transfer logic
- c) Register transfer level
- d) Resistor-transistor logic

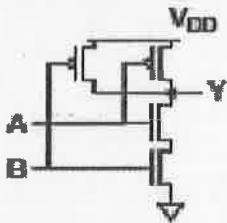
7. Simulator enters in which phase after the initialization phase?

- a) Execution phase
- b) Compilation phase
- c) Elaboration phase
- d) Simulation phase

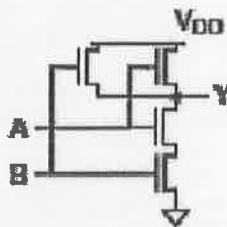
8. Conversion of RTL description to Boolean _____ description is a function of the translation procedure in the synthesis process.

- a) Optimized
- b) Unoptimized
- c) Translation
- d) PLA format

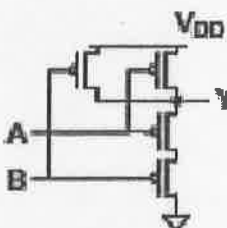
9. The CMOS logic circuit for NAND gate is:



a)



b)



c)

d) None of the mentioned



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10. In CMOS logic circuit the n-MOS transistor acts as:
- Load
 - Pull up network
 - Pull down network
 - Not used in CMOS circuits
11. RTL is used in HDL to create what level of representations in the circuit?
- High-level
 - Low-level
 - Mid-level
 - Same level
12. Which of the following tool performs logic optimization?
- Simulation tool
 - Synthesis tool
 - Routing tool
 - RTL compiler
13. When both nMOS and pMOS transistors of CMOS logic design are in OFF condition, the output is:
- 1 or Vdd or HIGH state
 - 0 or ground or LOW state
 - High impedance or floating(Z)
 - None of the mentioned
14. Which type of CPLD packaging comprises pins on all four sides that wrap around the edges of chip?
- Plastic-Leaded Chip Carrier (PLCC)
 - Quad Flat Pack (QFP)
 - Ceramic Pin Grid Array (PGA)
 - Ball Grid Array (BGA)
15. Which among the following is an output generated by synthesis process?
- Attributes & Library
 - RTL VHDL description
 - Circuit constraints
 - Gate-level net list
16. Why do we need concurrent processing for describing digital systems in HDLs?
- Complexity of digital systems needs concurrent processing
 - Faster processing than conventional programming languages
 - Concurrent processing is easier than sequential processing
 - It allows taking timing constraints into consideration



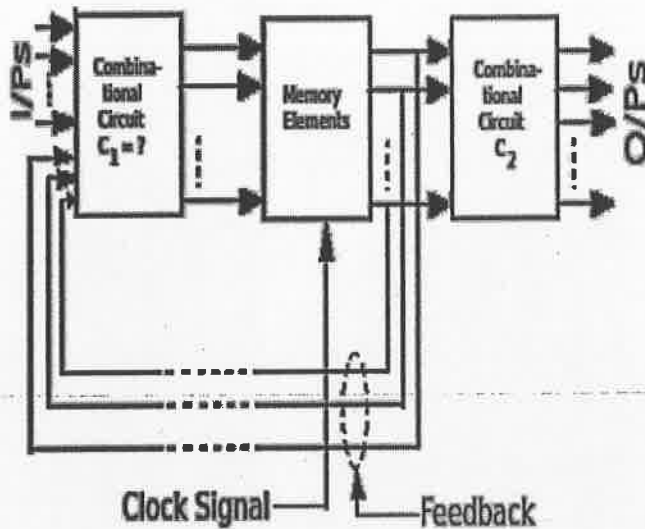
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17. From the generalized schematic of Moore circuit given below, what does the combinational circuit 'C₁' known as?



- a) Previous state decoder
- b) Present state decoder
- c) Next state decoder
- d) Output state decoder

18. In CMOS logic circuit the p-MOS transistor acts as:

- a) Pull down network
- b) Pull up network
- c) Load
- d) Short to ground

19. A counter circuit is usually constructed of _____

- a) A number of latches connected in cascade form
- b) A number of NAND gates connected in cascade form
- c) A number of flip-flops connected in cascade
- d) A number of NOR gates connected in cascade form

20. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

- a) 0 to 2^n
- b) 0 to $2^n + 1$
- c) 0 to $2^n - 1$
- d) 0 to $2^{n+1/2}$



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21. In CMOS logic circuit, the switching operation occurs because:
- Both n-MOSFET and p-MOSFET turns OFF simultaneously for input '0' and turns ON simultaneously for input '1'
 - Both n-MOSFET and p-MOSFET turns ON simultaneously for input '0' and turns OFF simultaneously for input '1'
 - N-MOSFET transistor turns ON, and p-MOSFET transistor turns OFF for input '1' and N-MOS transistor turns OFF, and p-MOS transistor turns ON for input '0'
 - None of the mentioned
22. If a port is declared as buffer, then which problem is generated in hierarchical design due to mapping with port of buffer mode of other entities only?
- Structural Modeling
 - Functional Modeling
 - Behavioral Modeling
 - Data Flow Modeling
23. Consider the state equation given below. If R.H.S of an equation is zero, then what would be the value of L.H.S (next state) after the application of a clock pulse?
- $$Q_{A(n+1)} = (Q_A Q_B + Q_A Q_B) X + Q_A Q_B$$
- Zero
 - Infinity
 - $Q_A Q_B X$
 - $Q_A Q_B X$
24. In Net-list language, the net-list is generated _____ synthesizing VHDL code.
- Before
 - At the time of (during)
 - After
 - None of the above
25. The output of sequential circuit is regarded as a function of time sequence of _____.
- Inputs
 - Outputs
 - Internal States
 - External States
- A & D
 - A & C
 - B & D
 - B & C


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Department of Electronics and Communication Engineering

Academic Year 2021-2022

Certificate Program on "RTL Design and Verification"

Assessment Result

S.NO	REGISTER NUMBER	STUDENT NAME	MARRKS
FINAL YEAR			
1	731218106001	BABY SHALINI G	92
2	731218106002	DEEPAK M	96
3	731218106003	DHARANI M	88
4	731218106006	JEEVITHA P	92
5	731218106009	KEERTHANA T	96
6	731218106013	PRIYA R	84
7	731218106014	PRIYA V	84
8	731218106015	PRIYADHARSINI A	68
9	731218106016	RAMACHANDHIRAN G	76
10	731218106017	SAKTHISUNDARAM D	80
11	731218106018	SANTHIYA A	72
12	731218106301	MANIVEL M	78
THIRD YEAR			
13	731219106001	BHARATHI M	84
14	731219106004	JAGADESHKUMAR G	78
15	731219106006	KEMPARAJ K	44
16	731219106008	MATHAN KUMAR M	64
17	731219106009	MOHAN K	96
18	731219106010	MUTHUPANDI M	92
19	731219106011	NANDHINI P	64
20	731219106012	NARMATHA M	72
21	731219106014	RAMESH PRABHU R	68
22	731219106015	ROHINI M	36
23	731219106016	SABARI GAYATHRI A	88
24	731219106018	SATHYAPRIYA K	92
25	731219106019	SURENDHAR P	84
26	731219106021	UDHAYAKUMAR M	78
SECOND YEAR			
27	731220106002	KALYAN K	92
28	731220106004	KUDIYARASU P	88
29	731220106005	MUTHUKUMAR M	84
30	731220106007	SUGUNA DEVI M	32
31	731220206301	JANARTHANAN K	92

Note : The students who secured 50 Marks and above are eligible to get certificates.


PROGRAM COORDINATOR


HOD


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T.N.Palayam(Po), Gobi(Tk), Erode(Dt) – 638 506



Department of Electronics and Communication Engineering

Academic Year 2021-2022

SUMMARY/OUTCOME REPORT

Name of the Certificate Program : RTL Design and Verification
Program Code : 21ECERTLDVCP01
Name of the Program Coordinator : Mrs.R.Kokila
Number of Students Enrolled : 31
Number of Students Completed : 28 Duration : 36 Hours

I hereby affirm that the entire program contents in the Certificate Program “RTL Design and Verification” listed in the certificate program Syllabus have been actually learned by the students as the part of the prescribed co-curricular activities through certificate program by NAAC and NBA.

I confirmed that the Certificate program title as RTL Design and Verification was done by me in the beginning of this semester and program delivery with attendance of the students were recorded.

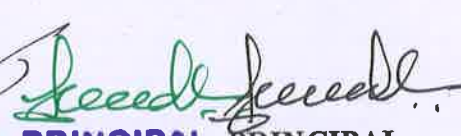
I confirmed that all registered students for this Certificate program were actively attended and performed well throughout the duration of this program. And all students were successfully completed and eligible to receive the participation certificate.

Outcome: Students shall able to gain knowledge in

- (i) An understanding of ASIC Design Flow, CMOS fundamentals, Advanced Digital Design, Verilog fundamentals.
- (ii) Learn different modelling styles and able to program using Verilog HDL.
- (iii) An understanding of RTL Design using Verilog and System Verilog.
- (iv) Able to perform RTL verification using Verilog and System Verilog.
- (iv) It gives foundation for FPGA design in Embedded Systems by using RTL schematic.


PROGRAM COORDINATOR


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CERTIFICATE OF PARTICIPATION

This is to certify that Mr./Ms.**MUTHUKUMAR M**.....of
.....**II - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**JANARTHANAN K**.....of
.....**II - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**KUDIYARASU P**.....of
.....**II - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**KALYAN K**.....of
.....**II - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**U.DHAYAKUMAR M**.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**SURENDHAR P**.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that ~~Mr./Ms.~~**SATHYA.....PRIYA.....K.....**.....of
.....**III - ECE.....**..... has successfully completed the certificate program titled "**RTL
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This is to certify that ~~Mr./Ms.~~**SABARI GAYATHRI A**.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**RAMESH PRABHU R**.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that ~~Mr./Ms.~~**N.ARMATHA M.**.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that ~~Mr./Ms.~~**NANDHINI P.**.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**MUTHU PANDI M**.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**MOHAN**.....k.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**MATHAN KUMAR M**.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**JAGADESKUMAR G**.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that ~~Mr./Ms.~~**B.HARATHI M**.....of
.....**III - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**MANIVEL M**.....of
.....**IV - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**SANTHIYA A**.....of
.....**IV - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**SAKTHISUNDARAM D**.....of
.....**IV - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**RAMACHANDHIRAN G**....of
.....**IV - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that ~~Mr./Ms.~~**PRIYA DHARSINI A**.....of
.....**IV - ECE**..... has successfully completed the certificate program titled "**RTL
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.....**IV - ECE**..... has successfully completed the certificate program titled "**RTL
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.....IV - ECE..... has successfully completed the certificate program titled "RTL
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This is to certify that ~~Mr./Ms.~~ **KEERTHANA . T** of
..... **IV - ECE** has successfully completed the certificate program titled "**RTL
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This is to certify that ~~Mr./Ms.~~ **JEEVITHA..P** of
..... **IV - ECE** has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**D.HARANI..M**.....of
.....**IV - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**DEEPAK M**.....of
.....**IV - ECE**..... has successfully completed the certificate program titled "**RTL
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This is to certify that Mr./Ms.**BABY SHALINI G**.....of
...**IV - ECE**..... has successfully completed the certificate program titled "**RTL
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