

Requisition Letter

From,

Head of the Department,
Department of Electronics and Communication Engineering,
J.K.K.Munirajah College of Technology,
T.N.Palayam.

To,

The Principal,
J.K.K.Munirajah College of Technology,
T.N.Palayam.

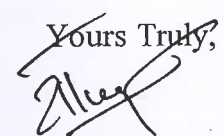
Permitted
12/1/23

Respected Sir,

Sub: Seeking permission for conducting a Certificate Program-Reg


We have planned to conduct a certificate program for II, III and IV-year ECE students on "FinFET Technology for Circuit Design" from 30.01.2023 to 04.02.2023 by program coordinator Mrs.B.P.Bright Thanga Mahizh AP/ECE. So, I request you to kindly provide permission to conduct the certificate program.

Thanking You,

Yours Truly,


Place: T.N.Palayam

Date: 12.01.2023


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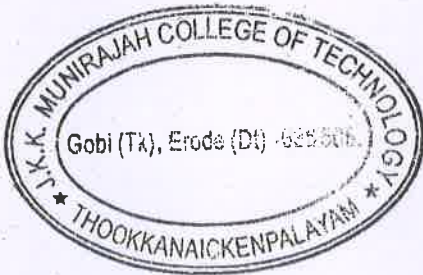


JKKMCT/CIRCULAR/21/JAN-2023

DATE: 13/01/2023

CIRCULAR

The Department of Electronics and Communication Engineering is planning to organize a Certificate Program on **"FinFET Technology for Circuit Design" (36 Hours)** for the benefit of the students from **30.01.2023 (Monday) to 04.02.2023 (Saturday)**. Students those who are willing to attend the program can enroll their names to their class in-charges respectively on or before 20.01.2023.



[Handwritten Signature]
13/1/23
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Copy To,

All the HODs and Staff Members,

The Student's circulation,

Notice boards and File copy

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Department of Electronics and Communication Engineering

PROGRAM SYLLABUS

Name of the Certificate Program : **FinFET Technology for Circuit Design**

Program Code : **22ECEFTCDP01**

Name of the Program Coordinator : Mrs.B.P.Bright Thanga Mahizh

Academic Year: 2022-2023

Program Contents

Total Hours: 36

Chapter 1 : Introduction to FinFET Technology

- Recap of semiconductor fundamentals
- Review of PN junctions, JFETs, and MOSFETs
- Evolution of MOSFETs to FinFETs
- Advantages and challenges of FinFET technology

Chapter 2 : FinFET Operation, Characteristics and Modeling

- FinFET background
- Evolution of MOSFETs to FinFETs
- Types of FinFET
- FinFET structure and fabrication
- Operational principles of FinFETs
- FinFET Advantages
- Applications of FinFET Technology
- Analyzing FinFET characteristics.
- Modeling FinFET behavior for circuit simulation

Chapter 3 : FinFET Circuit Design

- Design considerations for FinFET-based circuits
- Applications of FinFETs in analog and digital circuits
- Scaling trends in FinFET technology
- Exploring the future developments in advanced semiconductor devices
- FinFETs in integrated circuits and system-on-chip (SoC) designs

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Chapter 4 : Low Power Circuit Design with FinFETs

- Importance of low-power circuit design in CMOS and FinFET technologies.
- Evolution of low-power design in advanced semiconductor devices.
- Power consumption, efficiency, and trade-offs specific to FinFET technologies.
- Principles of advanced low-power design strategies in FinFET technologies
- Techniques for minimizing power consumption in digital and analog circuits with advanced semiconductor technologies

Chapter 5 : Energy-Efficient Components and Architectures in FinFETs

- Identification of energy-efficient components and circuit architectures specific to CMOS and FinFET technologies.
- Analyzing the impact of component selection on power efficiency in advanced semiconductor designs
- Hands-on exercises with energy-efficient components in FinFETs.
- Overview of simulation tools specific to advanced semiconductor technologies for analyzing and validating power performance.
- Hands on project

Prepared by:

Name: Mrs. B.P.Bright Thanga Mahizh
Designation: AP/ ECE

PROGRAM COORDINATOR

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Department of Electronics and Communication Engineering



Academic Year 2022-2023


Certificate Program on "FinFET Technology for Circuit Design"

Schedule Plan

Dates	09:30 AM to 11:30AM (2 Hrs)		11.45 AM to 1.15 PM (1.30 Hrs)		2:00 PM to 4.30 PM (2.30 Hrs)
30.01.2023	Review of Semiconductor Physics and Traditional Electronic Devices	BREAK	Introduction to FinFET Technology	LUNCH	FinFET Device Structure and Operation
31.01.2023	FinFET Characteristics and Modeling		FinFET Circuit Design		Applications of FinFETs in analog and digital circuits
01.02.2023	FinFET Scaling and Future Trends		FinFETs in integrated circuits and system-on-chip (SoC) designs		Importance of low-power circuit design in FinFET technologies
02.02.2023	Power consumption, efficiency, and trade-offs specific to FinFET technologies		Principles of advanced low-power design strategies in FinFET technologies		Techniques for minimizing power consumption in digital and analog circuits with advanced semiconductor technologies
03.02.2023	Simulation exercises focusing on low-power techniques with FinFETs		Identification of energy-efficient components and circuit architectures specific FinFET technologies		Analyzing the impact of component selection on power efficiency in advanced semiconductor designs
04.02.2023	Overview of simulation tools specific to advanced semiconductor technologies for analyzing and validating power performance		Hands-on training with simulation software tailored FinFET designs		Hands on training Questions and feedback


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Department of Electronics and Communication Engineering

Academic Year 2022-2023

Resource Person Profile

Title of the Program	FinFET Technology for Circuit Design
Duration and Timing of the Program	36 Hours & 9.30 AM to 4.30 PM
Name of the Resource Person	Mrs.B.P.Bright Thanga Mahizh
Photo Image of the Resource Person	
E-mail	bpmahizh@gmail.com
Mobile No	6380675207
Designation	Assistant Professor / ECE
Official Address	Department of ECE, J.K.K.Munirajah College of Technology, T.N.Palayam, Gobi(tk), Erode(Dt) - 638506
Educational Qualification	B.E (Electronics and Communication Engineering), M.Tech (Applied Electronics)
Experience	Eight years of Teaching experience as an assistant professor in our college.
Field of Interest	Electronic Devices, Digital Signal Processing, VLSI Design, Electromagnetic Field


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Department of Electronics and Communication Engineering
Academic Year 2022-2023
Certificate Program on "FinFET Technology for Circuit Design"
Students Willing List

S.NO	REGISTER NUMBER	STUDENT NAME	WILLING STUDENTS SIGNATURE
FINAL YEAR			
1	731219106001	BHARATHI M	M. Bhuy.
2	731219106004	JAGADEESH KUMAR G	G. Jagadeesh Kumar
3	731219106006	KEMPARAJ K	Kemparaj
4	731219106008	MATHANKUMAR M	M. Math
5	731219106009	MOHAN K	K. Mohan
6	731219106010	MUTHUPANDI M	M. Muthu
7	731219106011	NANDHINI P	P. Nandhini
8	731219106012	NARMATHA M	M. Narmatha
9	731219106014	RAMESHPRABHU R	R. Ramesh Prabhu
10	731219106015	ROHINI M	M. Rohini
11	731219106016	SABARIGAYATHRI A	A. Sabarigayathri
12	731219106018	SATHYA PRIYA K	K. Sathya Priya
13	731219106019	SURENDAR P	P. Surendar
14	731219106021	UDHAYAKUMAR M	M. Udhayakumar
15	731219106301	KURALARASAN D	Not willing
THIRD YEAR			
16	731220106002	KALYAN K	K. Kalyan
17	731220106004	KUDIYARASU P	P. Kudiyarasu
18	731220106005	MUTHUKUMAR M	M. Muthukumar
19	731220106007	SUGUNA DEVI M	M. Suguna Devi
20	731220106008	VIKRAM V	V. Vikram
21	731220106301	JANARTHANAN K	K. Janarthanan
SECOND YEAR			
22	731221106004	KAVIYA K	K. Kaviya
23	731221106006	MAHALINGAM S	S. Mahalingam
24	731221106007	NARMATHA M	M. Narmatha
25	731221106008	RANJITH B	B. Ranjith

S.NO	REGISTER NUMBER	STUDENT NAME	WILLING STUDENTS SIGNATURE
26	731221106009	SAKTHISIVAN K	K. Sakthisivan
27	731221106010	SANTHIYA Y	Santhiya. Y
28	731221106011	SATHASIVAN R	R. Satha Sivan
29	731221106012	SHARMILA V	sharmila. V
30	731221106014	SUBASH K	Subashk
31	731221106015	VENEESWARI M	M. Veneeswari
32	731221106301	ARTHI V	V. Arthi
33	731221106302	SHARMILA V	V. Sharmila
34	731221106303	SOUNDARIYA S	S. Soundariya



PROGRAM COORDINATOR



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Department of Electronics and Communication Engineering

Academic Year 2022-2023

Certificate Program on "FinFET Technology for Circuit Design"

Enrolled Students Name List

S.NO	REGISTER NUMBER	STUDENT NAME
FINAL YEAR		
1	731219106001	BHARATHI M
2	731219106004	JAGADEESH KUMAR G
3	731219106006	KEMPARAJ K
4	731219106008	MATHANKUMAR M
5	731219106009	MOHAN K
6	731219106010	MUTHUPANDI M
7	731219106011	NANDHINI P
8	731219106012	NARMATHA M
9	731219106014	RAMESHPRABHU R
10	731219106015	ROHINI M
11	731219106016	SABARIGAYATHRI A
12	731219106018	SATHYA PRIYA K
13	731219106019	SURENDAR P
14	731219106021	UDHAYAKUMAR M
THIRD YEAR		
15	731220106002	KALYAN K
16	731220106004	KUDIYARASU P
17	731220106005	MUTHUKUMAR M
18	731220106007	SUGUNA DEVI M
19	731220106008	VIKRAM V
20	731220106301	JANARTHANAN K
SECOND YEAR		
21	731221106007	NARMATHA M
22	731221106008	RANJITH B
23	731221106009	SAKTHISIVAN K
24	731221106010	SANTHIYA Y
25	731221106011	SATHASIVAN R
26	731221106012	SHARMILA V
27	731221106014	SUBASH K
28	731221106015	VENEESWARI M
29	731221106301	ARTHI V
30	731221106302	SHARMILA V
31	731221106303	SOUNDARIYA S

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Department of Electronics and Communication Engineering

Academic Year 2022-2023

Certificate Program on "FinFET Technology for Circuit Design"

Attendance Details

S.NO	NAME OF THE STUDENT	ATTENDANCE OF THE PARTICIPANTS											
		30.01.2023		31.01.2023		01.02.2023		02.02.2023		03.02.2023		04.02.2023	
		FN	AN	FN	AN	FN	AN	FN	AN	FN	AN	FN	AN
FINAL YEAR													
1	BHARATHI M	/	/	/	/	/	/	/	/	/	/	/	/
2	JAGADEESH KUMAR G	/	/	/	/	/	/	/	/	/	/	/	/
3	KEMPARAJ K	/	/	/	a	/	/	/	/	/	/	/	/
4	MATHANKUMAR M	/	/	/	/	/	/	/	/	/	/	/	/
5	MOHAN K	/	/	/	/	/	/	/	/	/	/	/	/
6	MUTHUPANDI M	/	/	/	/	/	/	/	/	/	/	/	/
7	NANDHINI P	/	/	/	/	/	a	/	/	/	/	/	/
8	NARMATHA M	/	/	/	/	/	/	/	/	/	/	/	/
9	RAMESHPRABHU R	/	/	/	/	/	/	/	a	/	/	/	/
10	ROHINI M	/	/	/	/	/	/	/	/	/	/	/	/
11	SABARIGAYATHRI A	/	/	/	/	/	/	/	/	/	/	/	/
12	SATHYA PRIYA K	/	/	/	/	/	/	/	/	/	/	/	/
13	SURENDAR P	/	/	/	/	/	/	/	/	/	/	/	/
14	UDHAYAKUMAR M	/	/	/	/	/	/	/	/	/	/	/	/
THIRD YEAR													
15	KALYAN K	/	/	/	/	/	/	/	/	/	/	/	/
16	KUDIYARASU P	/	/	/	/	/	/	/	/	/	/	/	/
17	MUTHUKUMAR M	/	/	/	/	/	/	/	/	/	/	/	/
18	SUGUNA DEVI M	/	/	/	/	/	/	/	/	/	/	/	/
19	VIKRAM V	/	/	a	a	/	a	a	a	a	/	/	/
20	JANARTHANAN K	/	/	/	/	/	/	/	/	/	/	/	/
SECOND YEAR													
21	NARMATHA M	/	/	/	/	/	/	/	/	/	/	/	/
22	RANJITH B	/	/	a	/	/	/	/	/	/	/	/	/
23	SAKTHISIVAN K	/	/	/	/	/	/	/	/	/	/	/	/
24	SANTHIYA Y	/	/	/	/	/	/	/	/	/	/	/	/
25	SATHASIVAN R	/	a	/	a	a	a	/	/	a	a	/	/
26	SHARMILA V	/	/	/	/	/	/	/	/	/	/	/	/
27	SUBASH K	/	/	/	/	a	/	/	a	/	/	/	/
28	VEEESWARI M	/	/	/	/	/	/	/	/	/	/	/	/
29	ARTHI V	/	/	/	/	/	/	/	/	/	/	/	/
30	SHARMILA V	/	/	/	/	/	/	/	/	/	/	/	/
31	SOUNDARIYA S	/	/	/	/	/	/	/	/	/	/	/	/
Total No. of Present		31	30	29	28	29	28	30	28	29	30	31	31
Total No. of Absent		Nil	01	02	03	02	03	01	03	02	01	Nil	Nil
Signature of Program Coordinator		/	/	/	/	/	/	/	/	/	/	/	/
Signature of HOD		/	/	/	/	/	/	/	/	/	/	/	/

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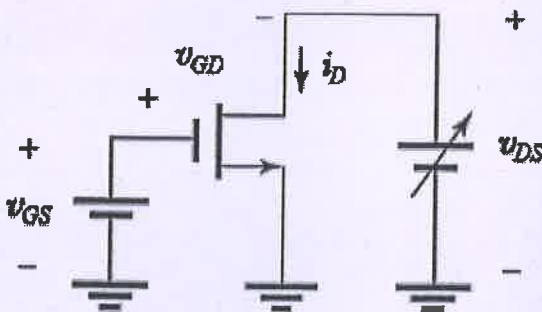


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Department of Electronics and Communication Engineering
Academic Year 2022-2023
Certificate Program on "FinFET Technology for Circuit Design"
Assessment Details

1. In Constant field model, the scaling factor of switching energy per gate would be:
 - a) $1/\beta \cdot \alpha^2$
 - b) $1/\alpha^3$
 - c) $1/\alpha^2$
 - d) All of the mentioned
2. The parameter which is not scaled to any factor is:
 - a) Power speed product
 - b) Switching energy
 - c) Channel resistance
 - d) All of the mentioned
3. If a MOSFET is to be used in the making of an amplifier then it must work in
 - a) Cut-off region
 - b) Triode region
 - c) Saturation region
 - d) Both cut-off and triode region can be used
4. Determine the conditions in which the MOSFET is operating in the triode region from the following figure.
 - i. $V_{GD} > V_t$ (Threshold voltage)
 - ii. $V_{DS} > V_{OV}$
 - iii. $I_D \propto (V_{OV} - 0.5V_{DS})V_{DS}$



- a) i, ii, and iii are correct
- b) i and iii are correct
- c) i and ii are correct
- d) ii and iii are correct



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5. Depletion layer of BSIM model is very thin because poly silicon gate is
- highly doped
 - lightly doped
 - not doped
 - neutral
6. FinFET was developed to overcome the
- short-channel effect
 - large-channel effect
 - mid-channel effect
 - no channel effect
7. SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an
- insulator
 - conductor
 - semiconductor
 - magnet
8. In SPICE, a sequence of nonlinear operating points calculated while sweeping an input voltage or current, or a circuit parameter analysis is
- AC analysis
 - DC analysis
 - DC transfer curve analysis
 - Noise analysis
9. FinFET is a
- Planar MOSFET
 - Non Planar MOSFET
 - Single gate MOSFET
 - No gate MOSFET
10. The initial step involved in the IC fabrication is _____.
- Silicon wafer preparation
 - Metallization
 - Ion implantation
 - Oxidation
11. FinFET generally used to design
- switch
 - amplifier
 - processors
 - integrator


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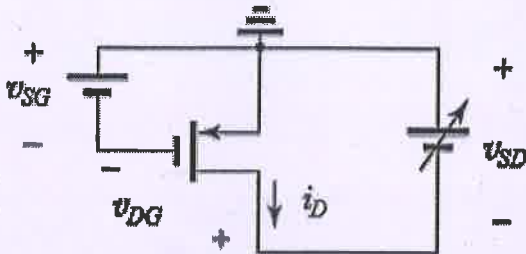
12. FinFET has low current drive which results in a

- a) zero gain
- b) high gain
- c) low gain
- d) 1/10 gain

13. Which of the following statements is true about extrinsic semiconductors?

- a) The gap between the conduction band and the valence band is more than 16 eV
- b) The gap between the conduction band and the valence band is about 1 eV
- c) The gap between the conduction band and valence band is 100 eV and more
- d) The conduction band and the valence band overlap.

14. The current i_D is?



- a) Depends linearly on V_{OV} in the saturation region
- b) Depends on the square of V_{OV} in the saturation region
- c) Depends inversely on V_{OV} in the triode region
- d) None of the mentioned

15. The extension of Moore's law is that computers, machines that run on computers, and computing power all become smaller and

- a) faster with time
- b) slower with time
- c) more power dissipation with time
- d) faster with frequency

16. The classification of ICs is also based on _____

- a) Presence of the active devices
- b) Number of transistors present
- c) None of the above
- d) All of above

17. SiO_2 is excellent at _____

- a) Dielectric
- b) Masking
- c) Insulating
- d) All the above

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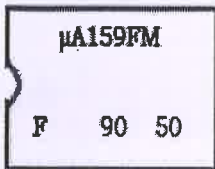


18. How a Motorola IC with plastic DIP and commercial temperature range is ordered?

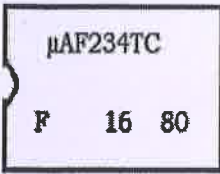
- a) ICLxxxP -> 0° to 75°c
- b) CAxxE -> -55° to +125°c
- c) LMxxxxA -> -40° to +85°c
- d) MCxxxP -> 0° to 70°c

19. Use device identification method to find the IC of Fairchild chip manufactured in the year 1980.

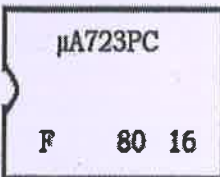
a)



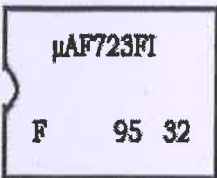
b)



c)



d)




20. FinFET exhibit more drive current per unit area than

- a) planar devices
- b) non planar devices
- c) dynamic devices
- d) static devices

21. What does the 1-2-3 numbering system used in National Semiconductor IC denotes

- a) Validity in years
- b) Temperature range
- c) Package type
- d) Ordering information


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22. How an eight pin Dual-In-Line Package is shortly named
- 8p DIP
 - Maxi DIP
 - Mini DIP
 - ES DIP
23. Find the ordering information for $\mu A741TC$.
- Sprague 741 DIP with Industrial temperature range
 - Intersil 741 DIP with commercial temperature range
 - Fairchild's 741 DIP with commercial temperature range
 - Texas instrument 741 metal can with Industrial temperature range
24. In BSIM model, threshold voltage of long channel device at zero substrate bias is termed as
- surface depletion voltage
 - inversion layer voltage
 - accumulation voltage
 - flat band voltage
25. FinFET operate at a lower voltage as a result of their
- lower drain voltage
 - lower threshold voltage
 - lower source voltage
 - lower gate voltage

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Department of Electronics and Communication Engineering
Academic Year 2022-2023
Certificate Program on "FinFET Technology for Circuit Design"
Assessment Result

S.NO	REGISTER NUMBER	STUDENT NAME	MARRKS
FINAL YEAR			
1	731219106001	BHARATHI M	88
2	731219106004	JAGADEESH KUMAR G	72
3	731219106006	KEMPARAJ K	70
4	731219106008	MATHANKUMAR M	82
5	731219106009	MOHAN K	96
6	731219106010	MUTHUPANDI M	92
7	731219106011	NANDHINI P	78
8	731219106012	NARMATHA M	88
9	731219106014	RAMESHPRABHU R	78
10	731219106015	ROHINI M	76
11	731219106016	SABARIGAYATHRI A	86
12	731219106018	SATHYA PRIYA K	94
13	731219106019	SURENDAR P	86
14	731219106021	UDHAYAKUMAR M	78
THIRD YEAR			
15	731220106002	KALYAN K	92
16	731220106004	KUDIYARASU P	88
17	731220106005	MUTHUKUMAR M	80
18	731220106007	SUGUNA DEVI M	74
19	731220106008	VIKRAM V	22
20	731220106301	JANARTHANAN K	94
SECOND YEAR			
21	731221106007	NARMATHA M	84
22	731221106008	RANJITH B	80
23	731221106009	SAKTHISIVAN K	82
24	731221106010	SANTHIYA Y	96
25	731221106011	SATHASIVAN R	36
26	731221106012	SHARMILA V	88
27	731221106014	SUBASH K	74
28	731221106015	VEEESWARI M	92
29	731221106301	ARTHI V	90
30	731221106302	SHARMILA V	86
31	731221106303	SOUNDARIYA S	84

Note : The students who secured 50 Marks and above are eligible to get certificates.


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Department of Electronics and Communication Engineering

Academic Year 2022-2023

SUMMARY/OUTCOME REPORT

Name of the Certificate Program : FinFET Technology for Circuit Design
Program Code : 22ECEFTCDP01
Name of the Program Coordinator : Mrs.B.P.Bright Thanga Mahizh
Number of Students Enrolled : 31
Number of Students Completed : 29 **Duration** : 36 Hours

I hereby affirm that the entire program contents in the Certificate Program "FinFET Technology for Circuit Design" listed in the certificate program Syllabus have been actually learned by the students as the part of the prescribed co-curricular activities through certificate program by NAAC and NBA.

I confirmed that the Certificate program title as FinFET Technology for Circuit Design was done by me in the beginning of this semester and program delivery with attendance of the students were recorded.


I confirmed that all registered students for this Certificate program were actively attended and performed well throughout the duration of this program and all students were successfully completed and eligible to receive the participation certificate.

Outcome: Students shall able to gain knowledge in

- (i) Analyze and describe the operation of traditional electronic devices such as PN junctions, JFETs and MOSFETs.
- (ii) Explore the principles and advantages of FinFET technology.
- (iii) Design and analyze FinFET-based circuits for specific applications.
- (iv) Develop an advanced understanding of low-power circuit design principles in the context of CMOS and FinFET technologies.
- (v) Identify energy-efficient components and circuit architectures specific to FinFET technologies.


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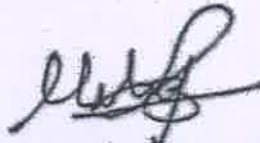
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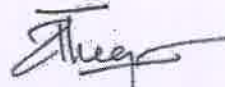
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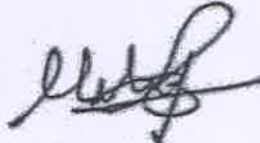
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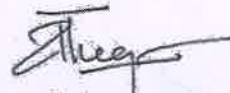
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This is to certify that Mr./Ms. KEMPARAJ K of
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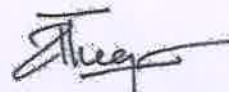
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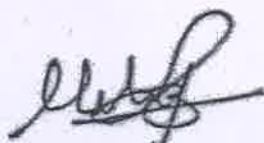
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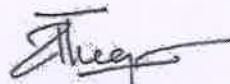
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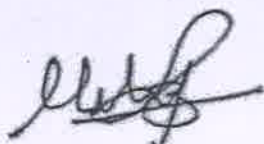
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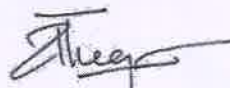
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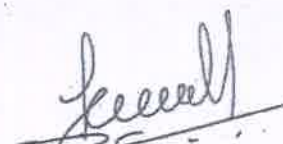
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This is to certify that Mr./Ms. KUDIYARASU P of
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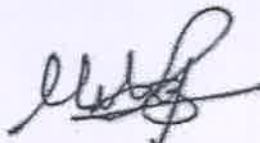
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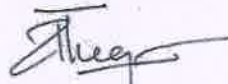
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This is to certify that Mr./Ms. SUGUNA DEVI M of
III - ECE has successfully completed the certificate program
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This is to certify that Mr./Ms. JANARTHANAN K of
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CERTIFICATE OF COMPLETION

This is to certify that Mr./Ms. SAKTHIVAN K of
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DURATION : 30.01.2023 TO 04.02.2023

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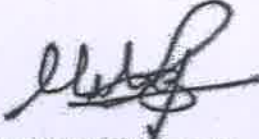
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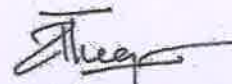
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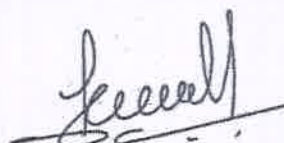
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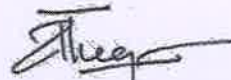
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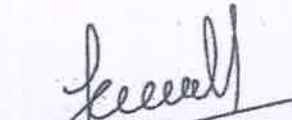
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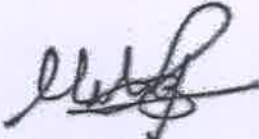
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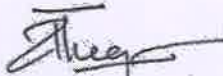
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